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NO. 375

A SURFACE AND AIR WEAPON INFORMATION SYSTEM FOR DDH-280 CLASS SHIPS (SAWIS-280)

Volume I

Introduction and Hardware Concept

by

J.F. Mickeal

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ABSTRACT

This report describes the hardware and software related concepts of SAWIS-280. A simplified description of the Surface and Air Weapons Control System is presented in the Introduction showing a need for a computer based performance monitoring/analysis system. Technical details of the relevant portions of the WM-22/6 Fire Control System are described as a base point for the design of two system interfaces. Also described in detail are the following: Fire Control Computer Interface, Auxiliary Equipment Interface and FCCI and AEI Control Software.

ACKNOWLEDGMENTS

Due to the extensive background and history leading up to the definition and realization of the SAWIS concept, it is impossible to name everyone involved.

However it should be recognized that the requirement for a SAWIS evolved through the combined efforts of Cdr. N.R.A. Smyth (DMCS); S. Abella and C. O'Higgins (DMCS-2); Combat System Engineers, Weapons and Fire Control Personnel (DDH-280 Class Destroyers); W.A. Jones and R.L. Campbell (DRES).

Within DRES, the author wishes to specifically acknowledge the invaluable assistance provided by D.N. Benson and N.A. Bannister in relation to the development of the entire hardware and related software concepts presented in this report.

For their continuous support during implemention of the SAWIS system the author wishes to acknowlege the efforts of the following groups;

a) Weapon System Group - W.A. Jones H/WSG, b) Computer Group - N.A. Bannister H/CG, c) Electronic Design Lab - D.R. Weiler H/EDG.

Through the continuing support of D. Little, H/EES and Dr. R.M. Heggie, C/DRES, SAWIS-280 will become a physically realizable entity.

In the preparation of this report the author would also like to acknowledge the efforts of Mrs. Barbara Ayling in relation to a very complex typing assignment.

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1. INTRODUCTION

SAWIS-280 is a computer orientated data acquisition/analysis system to be integrated into the WM-22/6 (abbreviated M-22) equipment of CRMS/GUN (close range missile/gun system) on DDH-280 class ships. The following is a simplified description of the M-22 system.

1.1 M-22 Equipment

Fig. 1.1 shows the configuration of the M-22 equipment. Input to the M-22 system is obtained from the radar set and optical sight. Two target tracking modes are possible, one air and one surface or shore. These may be done simultaneously, one by the port system and one by the starboard system.

For air tracking acquisition, the radar set indicates by means of a search antenna, the direction of the target. An operator aligns the tracking antenna in that direction. If a "lock on" is achieved, the target is automatically followed and its range and direction is presented to the fire control computer. The target is also illuminated by a CW signal for missile guidance purposes.

For surface tracking acquisition, the search portion of the radar is used to present directional information to the computer. The optical sight can provide target tracking information if required.

Having successfully acquired a target, an attack may be brought about by means of a Seasparrow AIM 7E2 surface to air missile and/or a 5"/54 cal. gun. There are two missile launchers, one on the port side and one on the starboard side. Each can fire up to 4 missiles sequentially. The 5"/54 cal. gun is mounted on the fo'c'sle of the ship.

The fire control computer interprets the available data on calculated target position, calculates a lead angle (the missile is aimed at the predicted point of intercept) based on the target's velocity and the ballistic properties of the missile, generates "head aim" values (to position a radar antenna in the missile towards the present target position) and english bias values (missile's initial course). These signals, which are continuously updated, are passed to the launcher servo system and missile. At operator command the missile is fired: other than target CW illumination, no further action by the M-22 system is taken. The missile has an internal guidance system which takes over to seek out the target.

Similarly a gun attack may be made. Ballistic equations for the particular type of shell used are employed by the computer to produce lead angles for the gun.

Note that in fig. 1.1 the relay box is used to assign the optical sight and gun to either the port or the starboard control system.

1.2 Need for SAWIS-280

The highly complex dynamic properties of this fire control/weapon system make evaluation of its performance (operational readiness, accuracy, deterioration, etc.) extremely difficult.

Approximately 200 signals (digital, analog and status) including target position, ship's own course, roll and pitch, operator control settings, mechanical failure indicators, error signals from launcher and gun, etc. must be recorded and analysed to achieve a meaningful report on the performance of the system.

DDH 280 class ships were not designed with an overall system monitoring capability, hence the need for SAWIS 280 to fill this role.

In figure 1.1, SAWIS-280 is shown connected to both the port and starboard M-22 equipments. Although several multisignal sources are shown, about 1/2 of the required signals are obtained from the fire control computer.

The following are the functions of SAWIS-280:

a) acquire and store intermediate data being manipulated by the M-22 fire control computer;

b) acquire and store significant status signals present in the M-22 system;

c) acquire and store significant analog signals present in the M-22 system;

d) input data into the M-22 fire control computer;

e) display any of the acquired data on a CRT terminal and create permanent copies of such data if desired;

f) assist in the analysis of acquired data by basic comparison and measurement tools such as graph manipulation, cursor measurement, etc.;

g) compute simulated target flight profiles to be inputted to the M-22 fire control computer for flight simulation purposes;

h) perform a self-analysis for verification of operation;

i) provide time correlation by a WWV synchronized clock.

1.3 SAWIS-280 Hardware

SAWIS-280 is hardware configured as shown in figure 1.2. A mil. spec. processor has been chosen in accordance with a move toward a standard shipboard computer by the Canadian Navy. The AN/UYK-20 (V) is an American military standard computer. All hardware and software options are stringently controlled by NAVELEX in Washington, D.C.. The processor was originally designed by Sperry-Univac, under a US Navy contract. Some of the features of the UYK-20 are:

- up to 64 K core memory;

- up to 32 general registers;

- DMA;

- Mathpack;
- Microprogrammable;
- Several I/O interface types;
- 16 I/O channels;
- software:
  - Disk Operating System
  - Assembler
  - Fortran
  - CMS-2M
  - SDEX - real time exec.

New USN standard peripherals and status reports on the UYK-20 are reported in "The Standard", a bi-monthly news letter published by NAVELEX.

SAWIS-280 on board ship will be configured as follows:

- UYK-20 processor;
- Dual Moving Head Disk;
- Tektronix RE4012 graphic display terminal;
- Tektronix R4610 hard copy unit;
- DRES designed M-22 interfaces.

Approximately 6 M words of data storage will be available on the Univac 1545-02 dual disk system. One cartridge is removable allowing the transportation of either an updated version of the software package or acquired data. Using the 3 M word removable disk for data storage, an acquisition run time of approx. 9 min can be achieved, allowing for the maximum data volume capacity of the SAWIS interface hardware. Longer run times (approx. 20 min) are possible if only one M-22 system (port or stbd) is accessed.

I/O such as acquisition software control commands, analysis control commands, graphs and graph measurement functions will be made via the Tektronix 4012 graphics display terminal. With its upper/lower case character set, it is ideally suited to display pages of reports detailing the performance of the M-22 system, including graphs. The 4610 hard copier will, by computer or manual control, provide permanent copies of such reports.

There will be two M-22 interfaces (fig. 1.2), one associated with the fire control computers (Fire Control Computer Interface - FCCI), the other accepting the status, clock, analog and digital data sources (Auxiliary Equipment Interface - AEI).

Initiated by the UYK-20, the AEI performs the following processing functions:

a) Status - A maximum of 160 status signals are compressed into ten 16 bit words. Each status source is isolated by an opto-isolator.

b) Analog - A maximum of 80(expandable to 256) analog signals, each pre-scaled, are multiplexed into an A/D converter. All analog channels have differential inputs to minimize ground loops.

c) Clock - Three 16 bit words of clock data are obtained from a WWV synchronized clock with a resolution of 0.01 sec.

d) External Digital Input - seven 16 bit words, for unspecified usage, e.g. video injection, RF frequency etc..

All processing functions and data transfers are controlled by the controller logic connected to I/O channel 10 of the UYK-20.

Passage of data to and from the fire control computers is the function of the Fire Control Computer Interface (FCCI). Since there are 2 fire control computers, port and starboard, for future reference various parts of the FCCI are duplicated while others are not. These are shown in figure 1.3.

By means of the FCCI, as the fire control computers execute instructions, intermediate data values, such as radar bearing, range, launcher bearing, etc. can be extracted or replaced by a set obtained from the UYK-20. Up to 48 such instructions (program counter values) can be stored in and recognized by the address recognition hardware. As each selected instruction is executed, the address recognition hardware commands the Acquisition Hardware and/or the DIU hardware (Digital Input Unit - derived from an existing device used to inject data directly into the fire control computer) to acquire and/or input a data word. The FCCI also contains all the necessary controller logic, to allow communication with the UYK-20 and its software.

1.4 SAWIS-280 Software

As shown in figure 1.4 all software modules will run under the control of the Level 2 operating system (NAVELEX supplied system software). Part of level 2, the I/O Executive, apart from controlling the two supplied peripherals (Disk & Tektronix 4012), will also control the FCCI & AEI hardware.

For the various types of trials (missile tracking, live missile firing, gun firing) different sets of signals will be acquired by SAWIS. Also, if required, different target flight profiles can be simulated by SAWIS. For each of these trials therefore, there exists a set of signals and a flight simulation equation that will apply.

In order to be able to define each trial conveniently through operator interaction with SAWIS software, the standard SAWS signal mnemonics will be used. The module, Define Signals, will enable an operator to define the equivalence of all signals used by SAWIS to their corresponding binary codes which relate to the operation of the AEI & FCCI interfaces. Addition or deletion of signal mnemonics will also be incorporated into Define Signals.

Definition of each trial will be made through the Define Trial Parameters module. Each trial is identified by a mnemonic with the following data entries:

a) FCCI signal list

b) AEI signal list

c) flight simulation equations

d) Real time display formatting

Real time display will allow the plotting of simple graphs of signals during a trial. The Trial Controller (figure 1.4) is responsible for directing the FCCI & AEI interfaces to do I/O data transfers related to the desired trial being run. For example, to perform a specific trial, an operator simply runs the Trial Controller, enters the trial mnemonic, then after some internal initialization based on the predefined specific trial, the controller will reply with "ready". The trial may then be initiated by simply entering a start command; acquired data will then be automatically stored on disk and the simulated flight data will be continuously injected into the M-22 computer (DIU operations). Termination of the trial can be made to occur by operator command or automatically when the data disk is filled.

If at any time (not during a trial) the value or state of any particular signal is required, running the Quick Look program with that particular signal mnemonic will result in the value or state to be displayed on the CRT terminal.

Several SAWIS system checkout programs will be available for diagnostics as well as a general GO/NO GO program.

After a trial has been completed, any signal may be examined in graphical form using the display module. Amplitude or time measurements may be taken by positioning the cursors (generated by the Tektronix 4012) over the significant points of the graph and entering a command to display the x - y value of the cursor.

The Analysis Package is an expandable module containing, initially, various analysis routines such as the plotting of the head aim error (the angular difference between the target position and missile seeker head position). A detailed description of the analysis modules will be a forthcoming publication.

The detailed definition of the SAWIS software will be available in SAWIS-280 Vol 2 in the near future.

1.5 SAWIS-280 Development

To enable the development of such complex software, a Program Generating Center (PGC), based at DRES, will consist of the shipboard peripherals previously described plus a card reader and line printer as shown in fig. 1.2. The reel to reel mag tape unit will be used for mass storage of data obtained from all 4 ships for performance correlation and history type analyses. The cartridge mag tape unit (CMTU) would provide a convenient software transportable medium but is not a requirement.

The following sections in this report may be used as reference material in the integration of various sections of the SAWIS prototype, as well as reference material for the integration of SAWIS-280 into the M-22 Weapon System.

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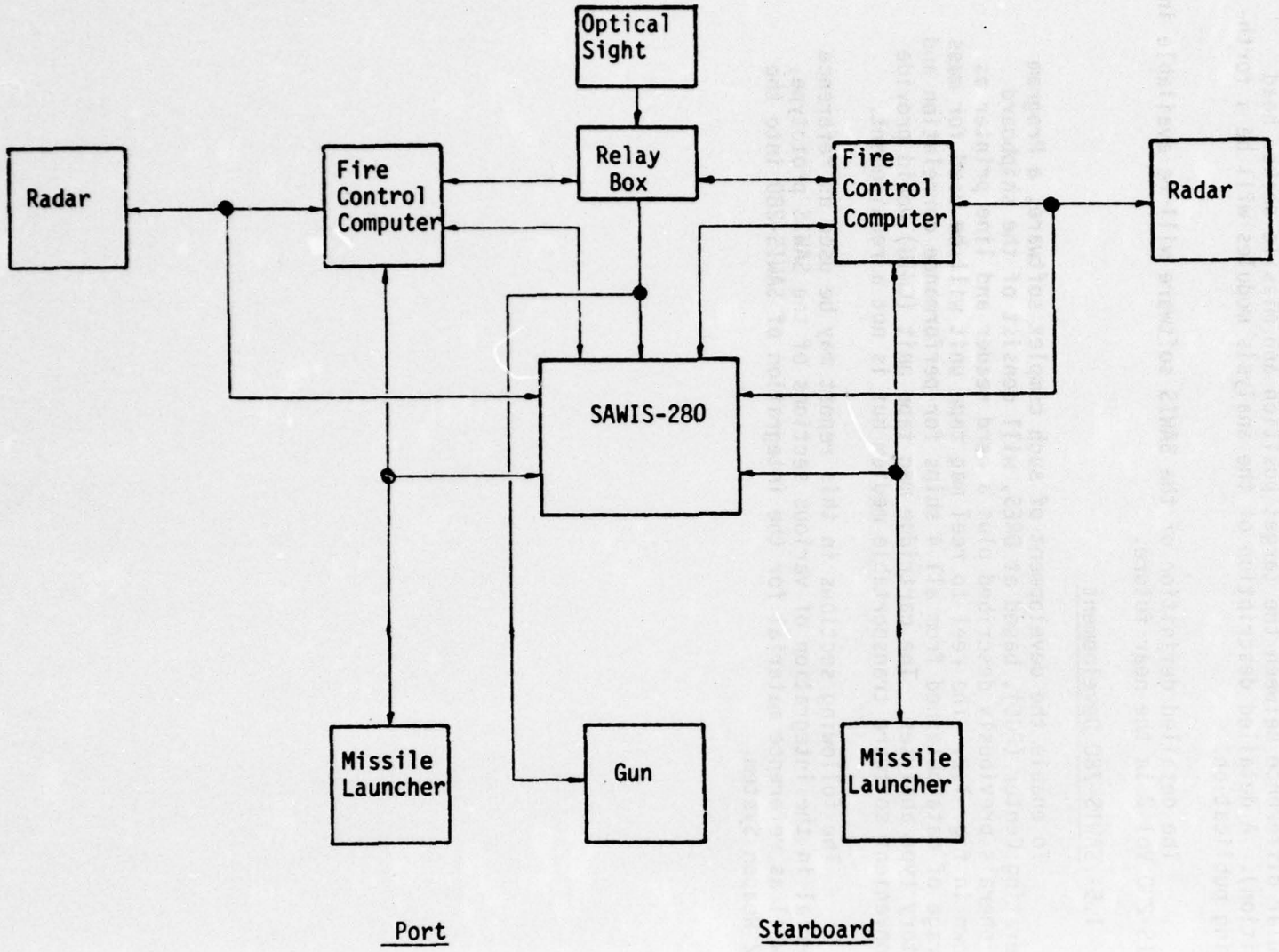

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Figure 1.1 SAWIS-280 Integration into the WM-22/6 Weapon System

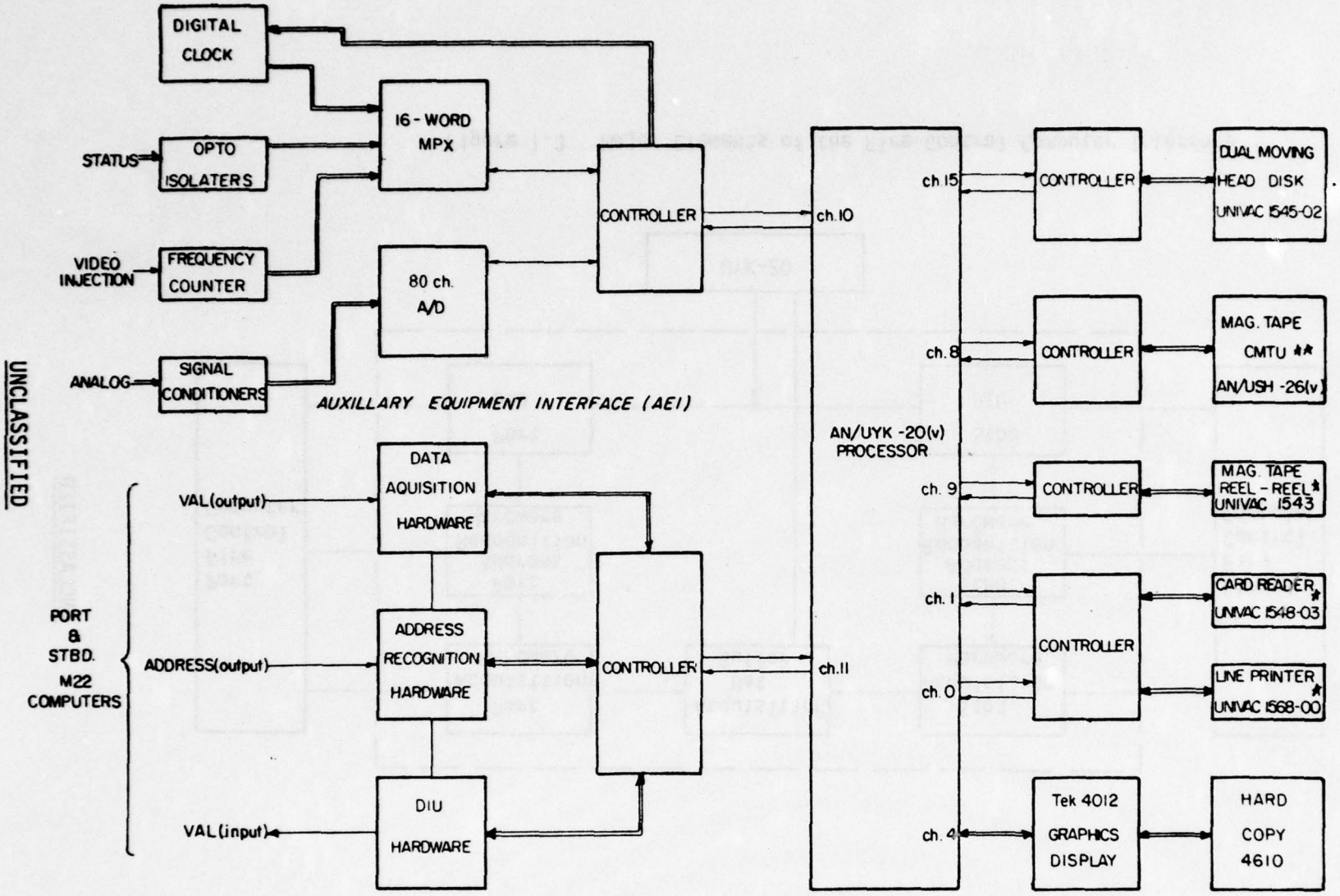

FIG. 1.2 SAWS-280 CONFIGURATION

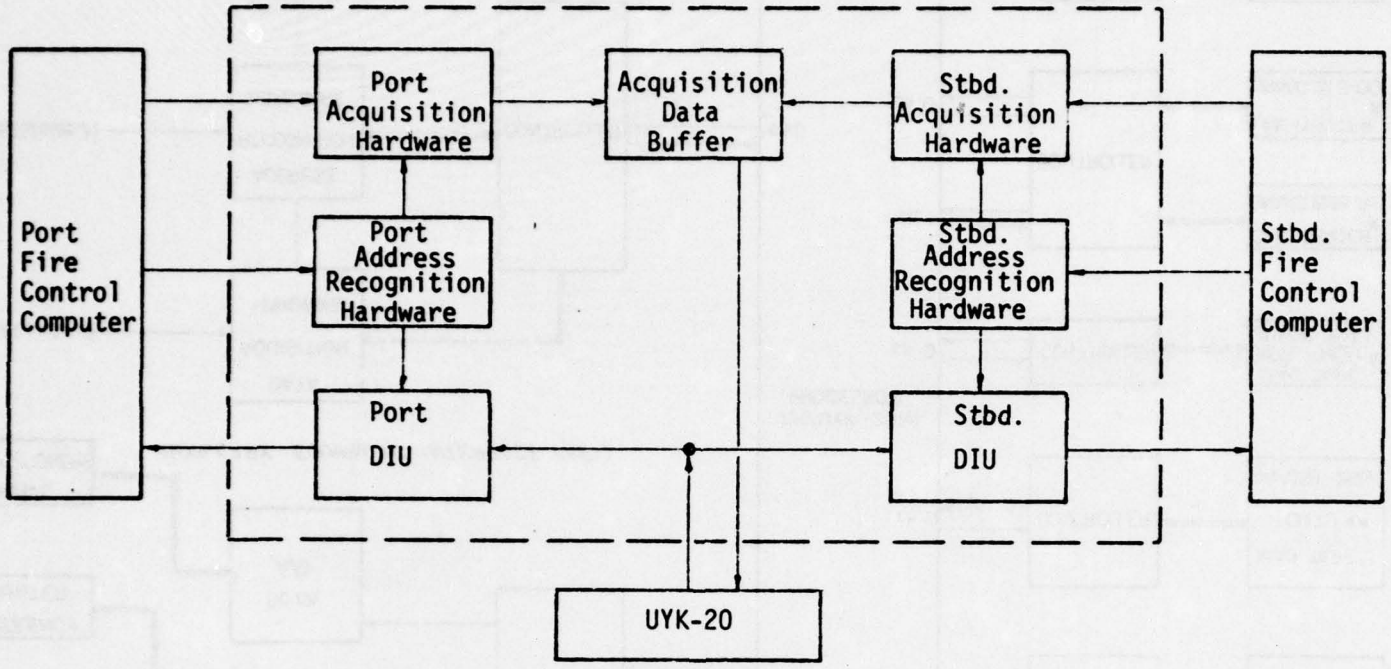

Figure 1.3 Major Elements of the Fire Control Computer Interface

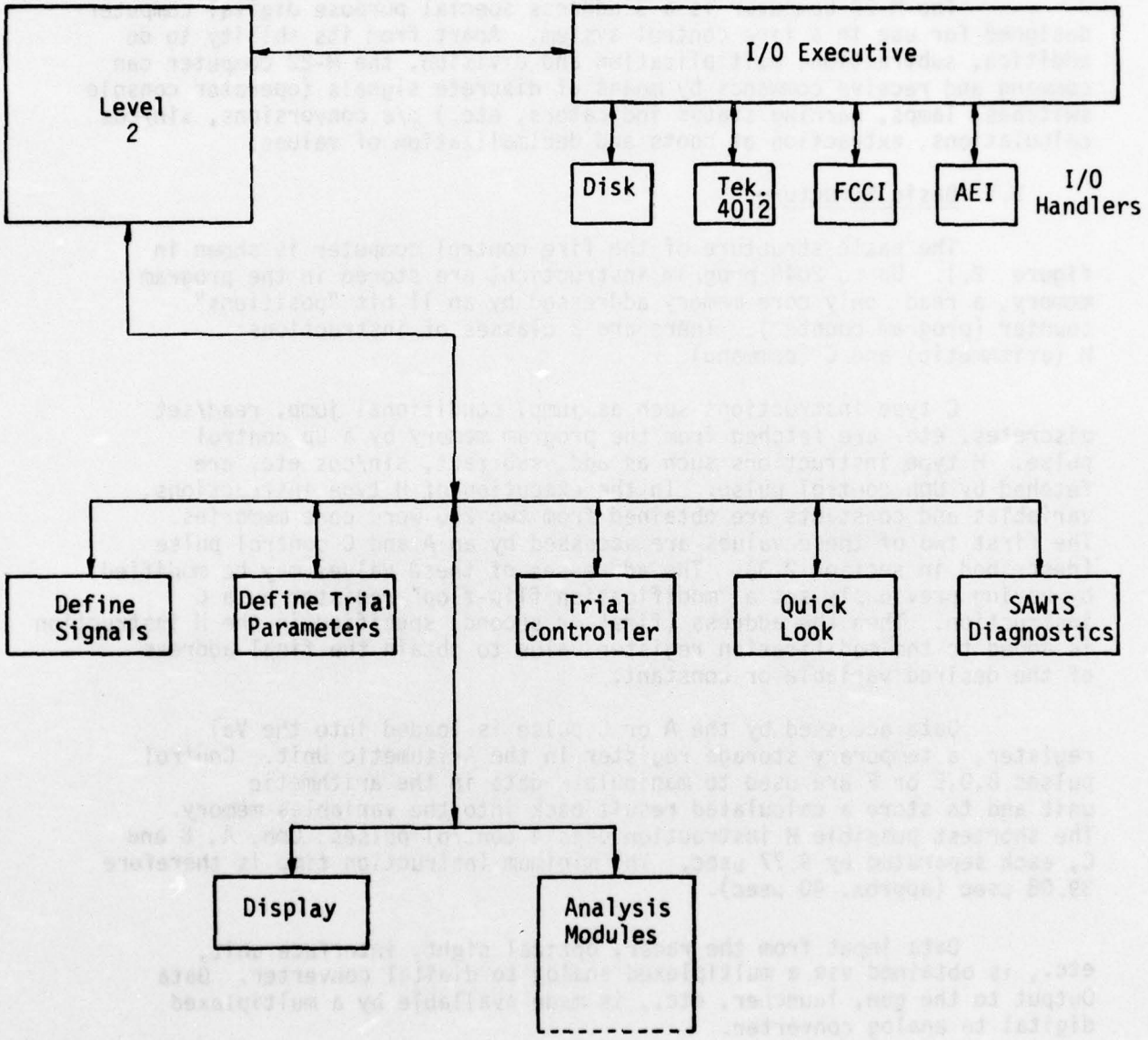

Figure 1.4 SAWIS-280 Software Modules

2. FIRE CONTROL COMPUTER

The M-22 Computer is a 3 address special purpose digital computer designed for use in a fire control system. Apart from its ability to do addition, subtraction, multiplication and division, the M-22 computer can command and receive commands by means of discrete signals (operator console switches, lamps, warning status indicators, etc.) ρ/ϕ conversions, sin/cos calculations, extraction of roots and decimalization of values.

2.1 Basic Structure

The basic structure of the fire control computer is shown in figure 2.1. Up to 2048 program instructions are stored in the program memory, a read only core memory addressed by an 11 bit "positions" counter (program counter). There are 2 classes of instructions: H (arithmetic) and C (command).

C type instructions such as jump, conditional jump, read/set discretes, etc. are fetched from the program memory by a Up control pulse. H type instructions such as add, subtract, sin/cos etc. are fetched by Uph control pulse. In the execution of H type instructions, variables and constants are obtained from two 256 word core memories. The first two of these values are accessed by an A and C control pulse (described in section 2.3). The addresses of these values may be modified by having previously set a "modification flip-flop" register by a C instruction. Then the address (first or second) specified in the H instruction is added to the modification register value to obtain the final address of the desired variable or constant.

Data accessed by the A or C pulse is loaded into the Val register, a temporary storage register in the Arithmetic Unit. Control pulses B,D,E or F are used to manipulate data in the arithmetic unit and to store a calculated result back into the variables memory. The shortest possible H instruction uses 4 control pulses: Uph, A, B and C, each separated by 9.77 μsec. The minimum instruction time is therefore 39.08 μsec (approx. 40 μsec).

Data input from the radar, optical sight, interface unit, etc., is obtained via a multiplexed analog to digital converter. Data Output to the gun, launcher, etc., is made available by a multiplexed digital to analog converter.

The recursive fire control program is divided into 16 rounds. A round consists of 3200 internal clock pulses. The period of the clock is 9.77 μsec. Thus, one round is completed in 1/32 sec. The round number is contained in a 4 bit rounds counter and can be tested by a particular C type instruction. Program branching can be facilitated in this manner, such that sections of the program can be executed only during one round or a combination of rounds. Any number of instructions can be associated with a particular round, of course, limited by the program memory size.

2.2 FCCI Connection Point

Data is extracted from or inputted to the fire control computer by the fire control computer interface connected to MS-1 and MS-2, two multi-pin connectors on the lower left side of the front of the computer. The signals available at MS-1 and MS-2 are given in Table 2.1 and 2.2 respectively. The following is a list of the required signals.

a) Positions Counter - 11 bits from MS-1, 4ST4 - MSB, to 1ST1 - LSB.

b) Rounds Counter - 4 bits from MS-1, 2RT1 - MSB, to 1RT1 - LSB.

c) Val Output - 24 bits from MS-1, Lt - sign bit, LO - MSB, to L22 - LSB

d) Val Input - 24 bits from MS-2, iLt - sign bit, iLO - MSB, to iL22 - LSB.

e) Modification flip-flops - 3 bits from MS-2, F1, F2 and F3.

f) Control Pulses - A,B,C, Uph, and K (clock pulse).

g) DIU control pulse - $\hat{iL}$

h) Memory Disable - $\overline{bg}$.

2.3 Timing

The timing for these signals is given in fig. 2.2. The Uph, A, B, and C control pulses are generated sequentially, but are available on separate lines. Instruction n, the n'th location in the program memory, is specified by the positions counter. The contents of location n are loaded into an instruction decoder by the Uph pulse. The positions counter is then incremented by 1 by the A pulse (in some instructions the positions counter is incremented, or changed by other control pulses - but not by the Uph pulse).

The contents specified by the first address is fetched from the variables or constants memory by the A pulse. The contents of that location appear on the Val output lines after T_2 (2.8 μsec) and remain stable until the rise of the B pulse. Similarly, the contents of the second address appears on the Val output lines 2.8 μsec after the C pulse.

During a DIU operation (external data input to the Val register), if for T_3 (6 μsec min) before and T_4 (2.4 μsec) after the rise of either the A or C pulse the $\overline{bg}$ line is made low, the contents of the first or second address of the variables or constants memory is not loaded into the Val register. Then if the iIL pulse is generated coincident with the A or C pulse, "first or second address" data present on the external Val input lines (MS-2 connector) will be loaded into the Val register.

By synchronization of the interface to these various control pulses, it is possible to extract or input data to any intermediate calculation performed by the fire control computer. Since some instructions are only executed during a particular round or combination of rounds, and since some have modified addresses, the rounds counter and modification flip-flops must be monitored. These, however, are always stable during the Uph pulse.

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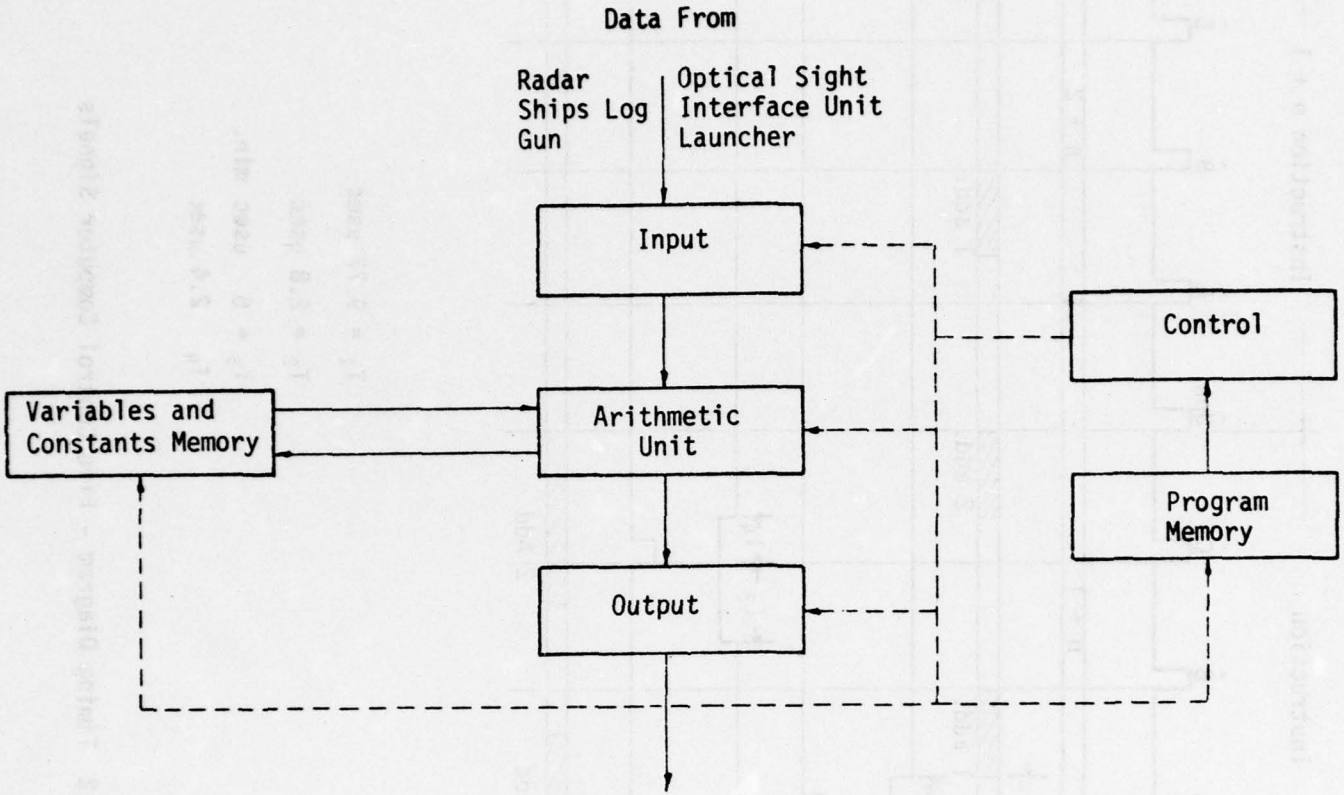

Figure 2.1 Basic Structure - Fire Control Computer

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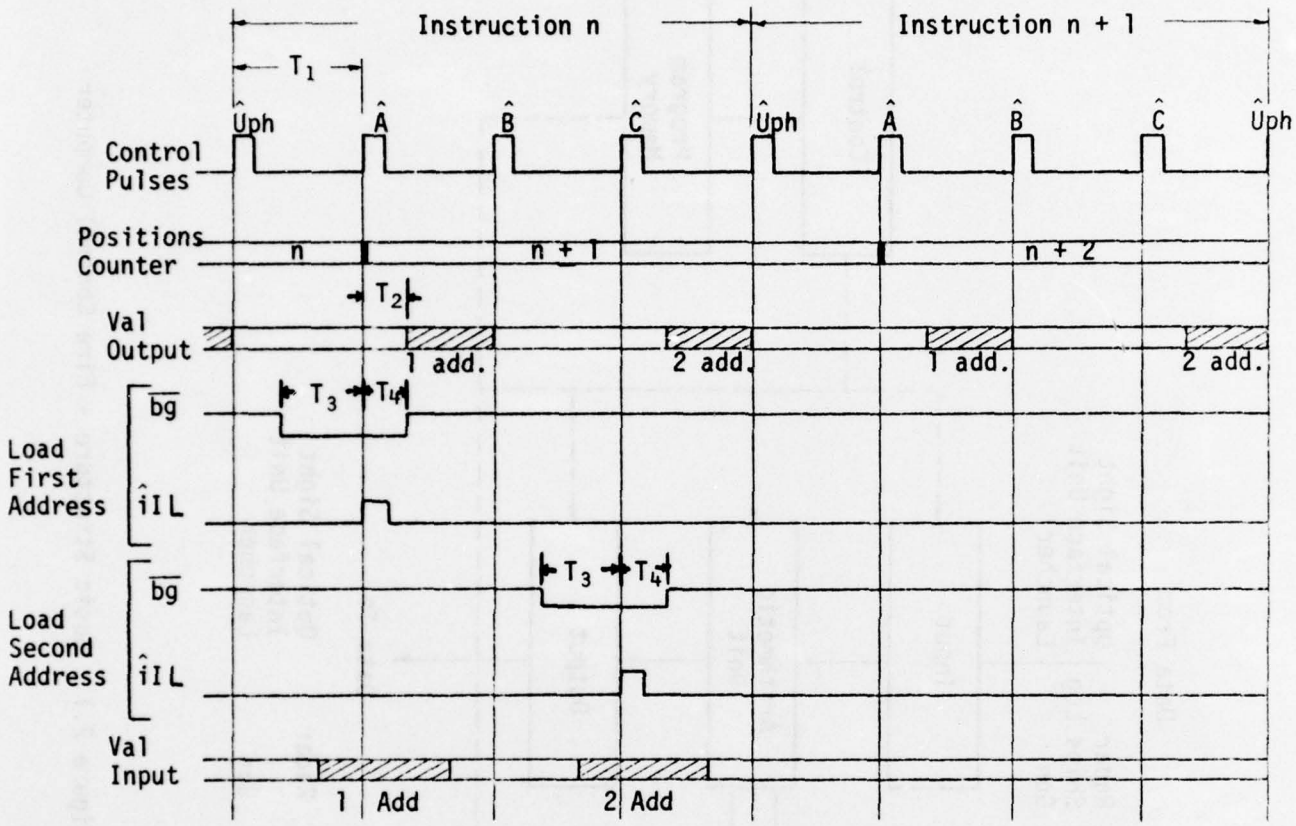


T_1 = 9.77 μsec

T_2 = 2.8 μsec

T_3 = 6 μsec min.

T_4 2.4 μsec

Figure 2.2 Timing Diagram - Fire Control Computer Signals

TABLE 2.1

MS-1

Pin No.	Computer Source	Function	Notes	Pin No.	Computer Source	Function	Notes
1				31	Y4/DD	F2	Mod FF
2				32			
3	W4/x	$\hat{K}$	Clock	33			
4		Shield		34	U3/A	Lt	-Sign bit
5				35	B	0	-MSB
6				36	C	1	
7				37	D	2	
8				38	E	3	
9				39	F	4	
10				40	H	5	
11				41	J	6	
12				42	K	7	
13	Y1/m	a		43	L	8	
14				44	M	9	Val
15	Y4/a	4ST4	-MSB	45	N	10	output.
16	c	4ST2		46	P	11	
17	e	4ST1		47	R	12	
18	h	3ST4		48	S	13	
19	k	3ST2	Positions	49	T	14	
20	n	3ST1	counter	50	U	15	
21	r	2ST2		51	V	16	
22	t	2ST1		52	W	17	
23	v	1ST4		53	X	18	
24	x	1ST2		54	Y	19	
25	Y4/y	1ST1	-LSB	55	Z	20	
26	Y5/k	2RT1	-MSB	56	a	21	
27	R1/x	1RT4	Rounds	57	U3/b	22	-LSB
28	R1/Z	1RT2	counter	58			
29	R1/b	1RT1	-LSB	59			
30	Y4/BB	F1	Mod FF	60			

TABLE 2.2

MS-2

Pin No.	Computer Source	Function	Notes	Pin No.	Computer Source	Function	Notes
1	W4/h	$\hat{A}$)	Control	31	Y4/FF	F3	Mod FF
2		Shield)		32	S4/v	$\overline{bg}$	Memory disable
3	W4/k	$\hat{B}$)	"	33	Y4/r	2ST2	Positions counter
4		)		34	S3/A	iLt	-Sign bit
5	W4/n	$\hat{C}$)	"	35	B	iL0	-MSB
6		)		36	C	1	
7	W4/r	$\hat{D}$)	"	37	D	2	
8		)		38	E	3	
9	W4/t	$\hat{R}$)	Clock	39	F	4	
10		)		40	H	5	
11	W4/v	$\hat{U}$ph)	Control	41	J	6	
12		)		42	K	7	
13	S6/FF	$\hat{i}$IL)	DIU control	43	L	8	
14		)		44	M	9	Val
15	Y4/a	4ST4	-MSB	45	N	10	Input
16	c	4ST2		46	P	11	
17	e	4ST1		47	R	12	
18	h	3ST4	Positions	48	S	13	
19	k	3ST2	counter	49	T	14	
20	n	3ST1		50	U	15	
21	t	2ST1		51	V	16	
22	v	1ST4		52	W	17	
23	x	1ST2		53	X	18	
24	z	1ST1	-LSB	54	Y	19	
25	R1/b	1RT1	-LSB	55	Z	20	
26	R1/z	1RT2	Rounds	56	a	21	
27	R1/x	1RT4	counter	57	S3/b	22	-LSB
28	Y5/k	2RT1	-MSB	58			
29	Y4/BB	F1	Mod.FF	59			
30	Y4/DD	F2	Mod.FF	60			

3. FIRE CONTROL COMPUTER INTERFACE - ADDRESS RECOGNITION HARDWARE

The signals presented at MS-1 and MS-2 contain all the information needed to determine any particular H type instruction that is being executed by the fire control computer. This data consists of:

a) 11-bit positions counter

b) 4-bit rounds counter

c) 3-bit modification register

and is stable from at least one clock pulse before the Uph pulse.

3.1 Address Memory

The address recognition hardware is capable of comparing each of 48 pre-stored addresses against the above signals. If a comparison is found, then the data acquisition or DIU hardware will be directed to acquire or input data to the M-22 computer. The structure of the address memory is shown in figure 3.1. DIU and/or Acquisition operations are associated with the first sixteen 32 bit words; Acquisition operations only are associated with the last thirty-two 16 bit words. The following is a definition of the various bit locations within the memory.

a) bit 31 - Address valid: 1 - address valid, allow a comparison to take place.
0 - disable comparators.

b) bit 30 - F-S Add: 0 - if a data transfer is to occur associated with a first (fire control computer) address.
1 - if a data transfer is to occur associated with a second address.

c) bits 19-29 - Positions Counter: 11-bit positions counter value associated with the data transfer.

d) bits 16-18 - Mod.FF: Contain the offset value which would be added to the first or second address within the fire control computer.

e) bits 11-15 - Rounds Count: Bit 15 = 1 (all) allows a DIU operation to occur on any round in which the specified instruction is found.
Bit 15 = 0 enables bits 11-14 (the 4-bit rounds count) to be compared with the rounds count lines from the computer.

f) bits 3-10 - Mod.FF Conditions: DIU or Acquisition is allowed for each correspondence of the 3 bit modification flip flop register with condition bits representing those values; (e.g. if bits 10, 8, 5 are set, DIU or Acquisition could occur for Mod.FF values of 7, 5 or 2).

g) bits 1-2 - A/DIU: Upon address recognition, Acquisition, DIU or both can occur according to the following code:

bit 2	bit 1	Function
0	0	A and DIU
0	1	A
1	0	DIU
1	1	A

h) bit 0 - 3MF/8MF: For Acquisition, bit 0 controls whether the 3 bit Mod.FF (logic 0) or the 8 bit Mod.FF conditions (logic 1) are to be compared. For DIU operations, the 8 MF section is always compared.

3.2 Data Transfers to and from the Address Memory

The address memory can be, upon command, loaded or read by the UYK-20 computer. Either of those commands, when issued, will cause a 64 word data transfer to or from corresponding 64 word UYK-20 core buffers to occur. The first 16 words of the address memory are arranged in upper and lower 16 bit bytes. Word 1 in the core buffer corresponds with the upper byte of word 1 in the address memory and word 2 corresponds with the lower byte. Thus the first 32 words of the core buffer contain data for the first 16 words of the address memory. There is a direct correspondence for the last 32 words, however.

If an address memory load command is issued to the hardware, the hardware generates 64 sequential data requests to the UYK-20, and after each request, stores the resulting data into the next sequential location or byte in the address memory. The UYK-20 I/O channel involved will have been previously initialized to refer to the address memory source buffer. Similarly, if a read command is issued, 64 words are transferred to the UYK-20 I/O channel.

These commands, and others such as Acquisition - port, DIU - starboard, etc., are issued to the hardware by program, and are accessible on the data lines of the I/O channel. A more detailed description of this process as well as that for the generation of a multi-source interrupt word will be given in section 6.

3.3 Address Recognition Examples

Assume, for the following examples, that the hardware has been given appropriate GO commands, and that it has been running for some time.

With reference to figure 3.2 comparison begins at each clock pulse preceeding a Uph pulse. Data from location 0 of the address memory is first compared against that from the computer, then data from location 1 etc., until the first 16 words of memory have been read. For a clock rate of 2.5 MHz this process is completed in T_2 = 6.4 μsec. At approximately the leading edge of the Uph pulse, the final 32 locations of the address memory are compared. Since T_3 could run up to 12.8 μsec, the value of the positions counter will have to be preserved beyond the A pulse. A hardware buffer is introduced here to latch the value of the required positions counter (n in figure 3.2) from the trailing edge of Kd_1, to the trailing edge of Kd_4. To effect this latched condition the trailing edge of each clock pulse is used to strobe the latch, except for the clock pulse corresponding to the A pulse. (Either the A, B or C pulse can increment the positions counter.) Thus during the critical time during which address comparisons are being made, the current positions counter value is guaranteed to remain unchanged.

Now consider the various address recognition operations that can take place. Assume that the address memory has been pre-loaded with the data for these examples.

a) Acquisition (from one of the first 16 locations of the memory - location 5).

- Fire Control Computer Instruction data.

  Positions Counter = 1234_8 = instruction n

  Mod. FF = 6_8

  Rounds Count = 15_8

- Contents of location 5

  AV = 1

  F/S Add = 0

  PC = 1234_8

Rounds Count = N/A (not DIU)

Mod. FF Cond. = N/A (not selected)

A/DIU - 01

3MF/8MF = 0

- Each of the locations of the address memory is compared by the following tests until a match is found. The match will be obtained during T_2, fig. 3.2, since this example has that data in location 5:

where subscripts FCC → fire control computer

AM → address memory

If: AV = 1

and: $PC_{FCC} = PC_{AM}$

$Mod.FF_{FCC} = Mod.FF_{AM}$

then: no further search of the Address memory is required; a match has been found.

Since: F/S Add = 0

A/DIU = 01

and: 3MF/8MF = 0

the Acquisition hardware will be instructed to acquire Val data associated with the first address of instruction n = 1234_8 for a Mod. FF value of 6_8 only.

- Had F/S add = 1, the second address Val data would be acquired.

b) DIU (from one of the first 16 locations - location 6).

- Fire Control Computer Instruction Data

Positions Counter = 1235_8

Mod. FF = 5_8

Rounds = 3_8

- Contents of Location 6

AV = 1

F/S Add = 0

PC = 1235_8

Mod. FF = N/A (DIU function)

Rounds Count = 3 ("All" bit = 0)

Mod. FF Cond. = 040_8 (bit 8 set)

A/DIU = 10

3 MF/8MF = N/A (DIU function).

Again, since location 6 will produce a match within T_2, the DIU hardware will be instructed to input data into the Val register when the following conditions have been tested.

If: AV = 1

and: $PC_{FCC} = PC_{AM}$

$Mod.\ FF_{FCC} = Mod.\ FF_{AM}$ (condition bits)

$Rounds_{FCC} = Rounds_{AM}$ (if "All" = 0)

Then no further search is required.

Since F/S Add = 0

A/DIU = 10

and: 3MF/8MF = N/A

the DIU hardware will be instructed to input data to the Val register associated with the first address of instruction 1235.

- Had F/S Add = 1, data would have been loaded into the Val register for the second address.

c) Acquisition and DIU (from location 7 of the address memory).

- Fire Control Computer Instruction Data

Positions Counter = 1236_8

Mod. FF = 2_8, 3_8, 5_8 (Acquisition on 3_8 only)

Rounds Count = N/A ("All" bit = 1)

- Contents of location 7

AV = 1

F/S Add - 0

PC = 1236_8

Mod. FF = 3_8

Rounds count = N/A ("All" bit = 1)

Mod. FF. Conditions = 054_8

A/DIU = 00

3MF/8MF = 0

The match will occur again within T_2 and the following conditions will be tested.

If AV = 1

and $PC_{FCC} = PC_{AM}$

Mod. FF_{FCC} = Mod. FF_{AM} (condition bits)

Then no further search is required.

Since: F/S Add = 0

A/DIU = 00

3MF/8MF = 0

the Acquisition hardware will be instructed to acquire data from the Val register during any round in which the instruction is found, but only when the Mod. FF address is 3. DIU will similarly occur but for Mod. FF values of 2,3, and 5.

- Had F/S Add = 1, the data transfers would have been associated with the second address.

- Had 3MF/8MF - 1, acquisition would have occurred for the same Mod. FF values as for the DIU.

d) Acquisition (from location 16 - 47).

Acquisition only (within T_3, figure 3.2) can occur for addresses stored in locations 16-47, where, if AV = 1, comparisons of the PC values and Mod. FF values (3 bits) are made.

3.4 Output Control and Data Transfers

In the preceding examples, the Acquisition and/or DIU hardware could be commanded to do data transfers. For reasons explained in the following sections describing these operations, the following data will have to be derived from the address recognition hardware. Note that at the time of an address match, the address memory is no longer incremented and its current location and contents are available for sampling.

a) Acquisition enable:

- Acquisition enable - a pulse synchronous with the condition of a correct (Acquisition type) address match.
- F/S address - from bit 30 of the current location of the address memory.
- AM location (6 bits) - the current location of the address memory that gave the address match.

b) DIU enable:

- DIU enable - a pulse synchronous with the condition of a correct (DIU type) address match.
- F/S address - from bit 30 of the current location of the address memory.
- AM location (6 bits) - the current location of the address memory that gave the address match.

Upon receiving an Acquisition or DIU enable pulse, the Acquisition or DIU hardware will read the above data and interact with the fire control computer for the appropriate data transfer.

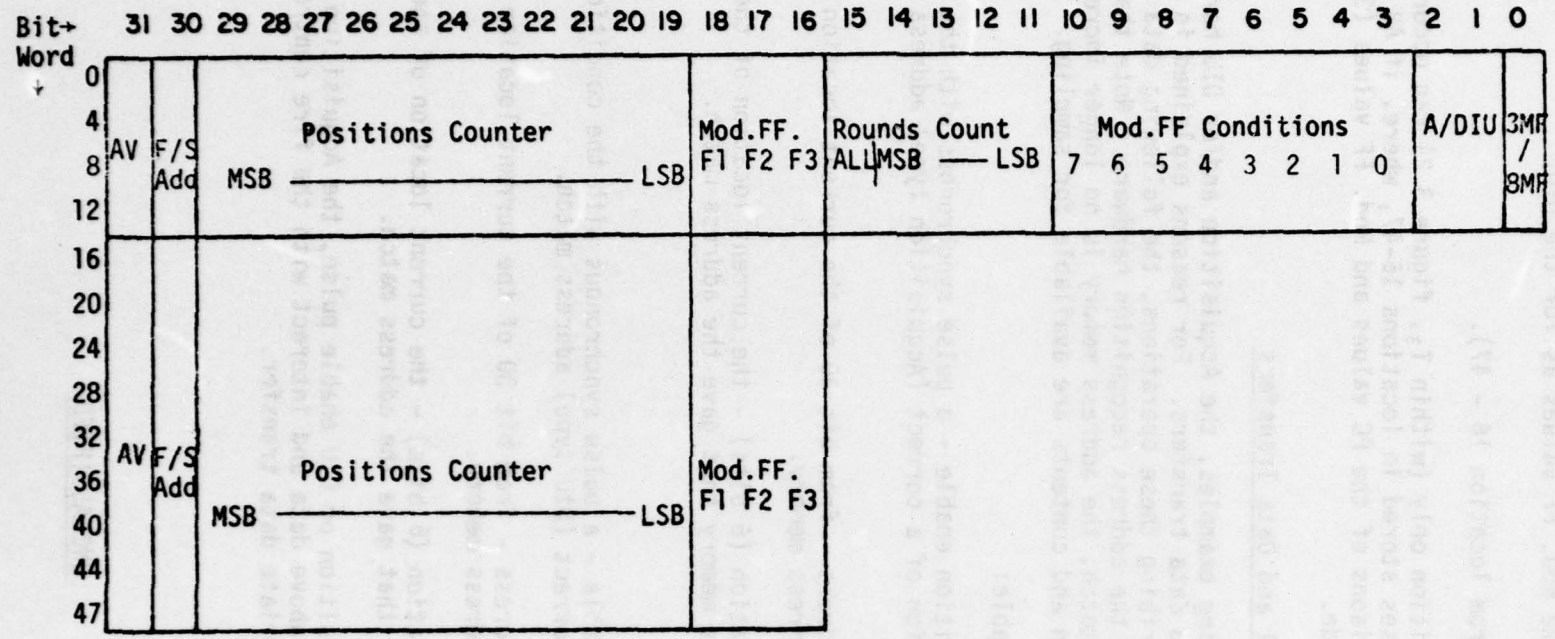
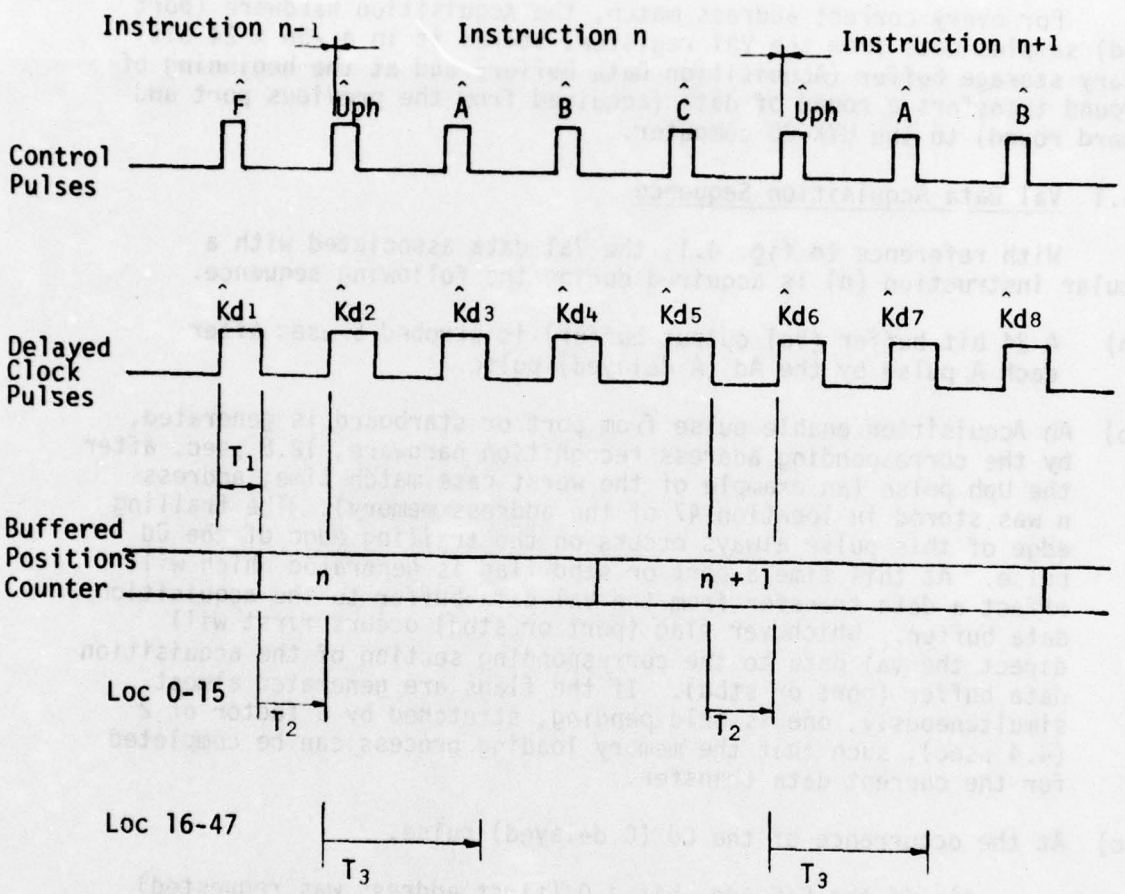


Figure 3.1 Address Memory Bit Definition



T_1 = 3μsec

T_2 = 6.4μsec max

T_3 = 12.8μsec max

Figure 3.2 Address Recognition Timing

4. FIRE CONTROL COMPUTER INTERFACE - ACQUISITION

For every correct address match, the Acquisition hardware (port or stbd) samples data from the Val register, stores it in a 256 x 24 bit temporary storage buffer (Acquisition Data Buffer) and at the beginning of each round transfers a round of data (acquired from the previous port and starboard round) to the UYK-20 computer.

4.1 Val Data Acquisition Sequence

With reference to fig. 4.1, the Val data associated with a particular instruction (n) is acquired during the following sequence.

a) A 24 bit buffer (Val output buffer) is strobed 5 μsec after each A pulse by the Ad (A delayed) pulse.

b) An Acquisition enable pulse from port or starboard is generated, by the corresponding address recognition hardware, 12.8 μsec. after the Uph pulse (an example of the worst case match time; address n was stored in location 47 of the address memory). The trailing edge of this pulse always occurs on the trailing edge of the Cd pulse. At this time a port or stbd flag is generated which will effect a data transfer from the Val data buffer to the acquisition data buffer. Whichever flag (port or stbd) occurs first will direct the Val data to the corresponding section of the acquisition data buffer (port or stbd). If the flags are generated almost simultaneously, one is held pending, stretched by a factor of 2 (4.4 μsec), such that the memory loading process can be completed for the current data transfer.

c) At the occurrence of the Cd (C delayed) pulse,

i) if the F/S add. bit = 0 (first address was requested)

- The Val output buffer is <u>not</u> restrobed by the Cd pulse (leaving the first address Val data available to be loaded into the Acquisition data buffer).

- This data is loaded into the Acquisition data buffer by the port or stbd. flag pulse.

ii) if the F/S add. bit = 1 (second address was requested)

- The Val output buffer <u>is</u> restrobed by the Cd pulse (now leaving the second address Val data available).

- The Acquisition data buffer is commanded to write this data into the appropriate location, again by the port or stbd flag pulse.

4.2 Acquisition Data Buffer

The Acquisition data buffer, figure 4.2, is divided into 4 fields, the Ap and Bp fields are for port acquisition data and the As and Bs fields are for starboard acquisition data. For addressing convenience, each field contains 64 words, although only the first 48 are used. Val data that is loaded into the memory is always stored in word lengths of 24 bits. Data transmitted to the UYK-20 may be either 16 or 24 bit words.

Figure 4.3 shows how the buffer is time shared. At the beginning of a rounds pulse, BORP or BORS (beginning of round port or stbd), the A and B buffers alternately become input buffers. While a particular buffer is being filled, the alternate one is dumped into the UYK-20. In figure 4.3, for example, during round n for the port side the Ap buffer is the input buffer and the Bp buffer (containing data from round n-1) is being dumped into the UYK-20.

Note: When the hardware is given a run command the A buffers will always become the input buffers when round 0 begins. (Acquisition will always start at the beginning of the first round 0 encountered after the run command.) Data from the B buffer is not valid during this first round 0, and therefore will not be sent to the UYK-20.

The memory is addressed by 8 bits, the least significant 6 of which are the relative address within a field. The next most significant bit defines the A/B field (0 for A, 1 for B) and the most significant bit defines the P/S block (0 for port, 1 for starboard). The first port or starboard flag pulse that appears due to an address match generates the following sequence:

a) The 6 address lines (AM location) from the corresponding port or starboard address memory are connected to the relative address lines of the buffer. (The address memory location where the match occurred had been saved at the time of the acquisition enable pulse.)

b) The corresponding A/B field bit which is changed every round for port or starboard is connected to the A/B field address line of the buffer.

c) The P/S block is selected by providing the P/S address line with a bit, the state of which corresponds to which Val data (Port or Starboard) is to be loaded.

d) The Port or Starboard Val data buffer is connected to the data lines of the buffer.

e) The Val data is written into the buffer.

Note: Steps a-d are performed at the leading edge of the flag pulse; step e starts at the trailing edge of the Cd pulse and continues for the time T_4. For a port-starboard sequential transfer when the first transfer is completed (e.g. port), then that flag is reset. The other flag (stbd asserted at the end of the T_4) effects the same storage operation (a through e) to store that Val data. The stbd flag is then reset.

If the port run command was issued, then the Ap buffer will be selected as the input buffer for port data at the beginning of a round. At the end of that round the Ap buffer will contain Val data in the same 48 locations as does the corresponding address memory data. Thus the Ap buffer may be sequentially dumped into the UYK-20, and the order will be preserved with no real time sorting required before the Val data is stored on disk. This will be described more clearly in section 8.

4.3 Priority and Timing

Since there are 3 operations, load-port, load-starboard and output, that can occur associated with the Acquisition data buffer, priority is given in the following manner:

a) Output data transfers are made word by word with a check for input requests between each transfer. Thus any input request is held pending for, at most, 2.2 μsec, the cycle time for one output transfer.

b) If both input requests and an output request occur simultaneously, the port input request is selected first, followed by the starboard, then the output request.

c) If during one input operation, the other generates a request, the second is serviced only after the completion of the first.

For a buffer memory cycle time of approximately 2.2 μsec, the worst case delay sequence is as follows:

d) At t = 0- the buffer is free and therefore an output operation is begun at t = 0.

e) At t = 0+ the port acquisition hardware generates an input request (at the trailing edge of the Cd pulse in figure 4.1).

f) At t = 0+ the starboard acquisition hardware generates an input request.

The resulting operations will take place:

g) The output operation will occur first, ending at t = 2.2 μsec.

h) Since port and starboard input requests occurred simultaneously the port operation is serviced first. Thus the memory, having previously been set up for port input, allows the load operation to begin at t = 2.2 μsec and terminates at t = 4.4 μsec, well before the port Val data buffer is restrobed at the next A pulse (the Val data is lost at the next A pulse). Thus, the port flag has been stretched by 2.2 μsec.

i) At T = 4.4 μsec the memory set up occurs for the starboard side. This is effected by asserting the stbd flag at T = 4.4 μsec. The stbd Val data is then loaded into the DM during the next 2.2 μsec, at which point the stbd flag is reset. This brings the total worst case delay to 6.6 μsec. However the stbd Val data is guaranteed to be valid at this time.

j) The buffer is now free to output more data to the UYK-20.

Note: Any data transfer from the DM is temporarily loaded into a 24 bit register. If a double word transfer to the UYK-20 is required, then this buffer is accessed twice (upper, then the lower 16 bit byte).

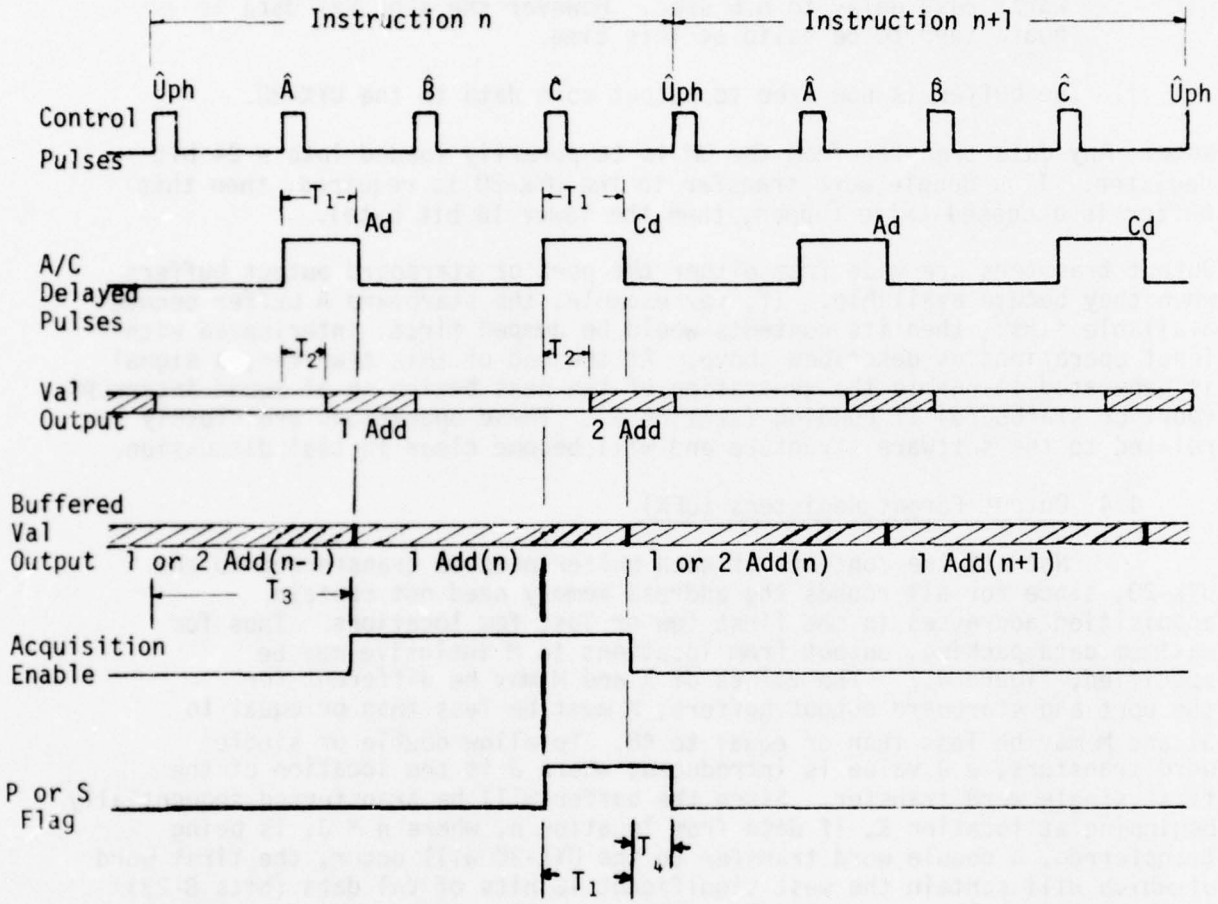
Output transfers are made from either the port or starboard output buffers when they become available. If, for example, the starboard A buffer becomes available first, then its contents would be dumped first, interleaved with input operations as described above. At the end of this transfer, a signal is generated to enable the generation of the next beginning of round interrupt (port or starboard) if pending (section 6). These operations are closely related to the software structure and will become clear in that discussion.

4.4 Output Format Registers (OFR)

Not all the contents of each buffer need be transferred to the UYK-20, since for all rounds the address memory need not contain acquisition addresses in the first few or last few locations. Thus for maximum data packing, output from locations to M inclusive may be specified, figure 4.2. The values of K and M may be different for the port and starboard output buffers, K must be less than or equal to 31 and M may be less than or equal to 48. To allow double or single word transfers, a J value is introduced, where J is the location of the first single word transfer. Since the buffer will be transferred sequentially, beginning at location K, if data from location n, where $n < J$, is being transferred, a double word transfer to the UYK-20 will occur, the first word of which will contain the most significant 16 bits of Val data (bits 8-23) in the buffer. The second word transferred will contain bits 0-8 of Val data in the upper byte. If $n \geq J$ or $J = 0$, then a single word transfer will occur, supplying the UYK-20 with the most 16 significant bits of Val data.

Note: For double word transfers, only one buffer cycle time is needed since all 24 bits are first loaded into a temporary register, before being transferred to the UYK-20.

The JKM values for the port and starboard are supplied by the UYK-20 before a run command is issued. These are loaded into 2 - 16 bit registers in the format shown in figure 4.4. The loading process will be described in Section 6.



T_1 = 5 µsec

T_2 = 2.8 µsec

T_3 = 12.8 µsec max.

T_4 = 2.2 µsec

Figure 4.1 Acquisition Timing

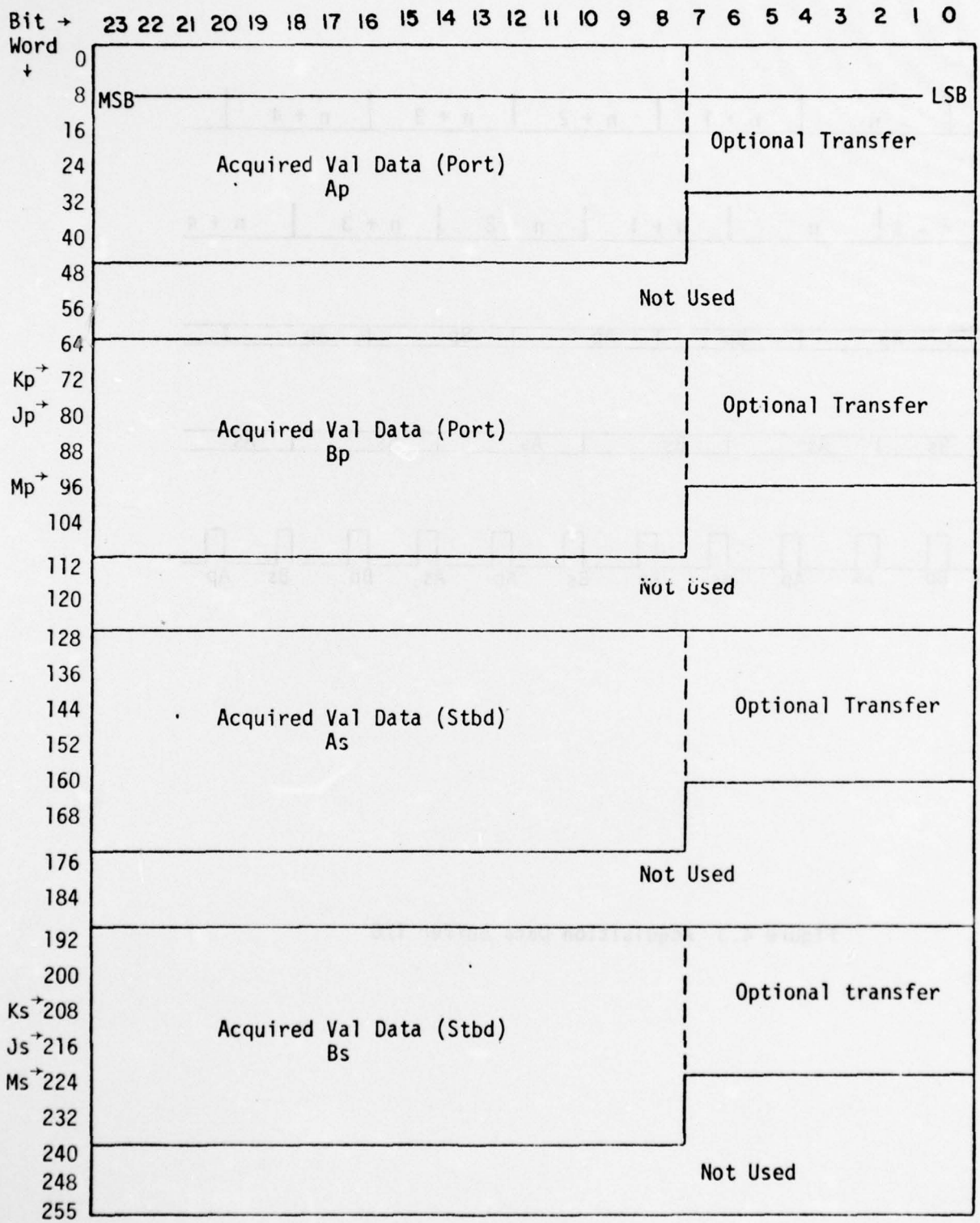


Figure 4.2 Acquisiton Data Buffer

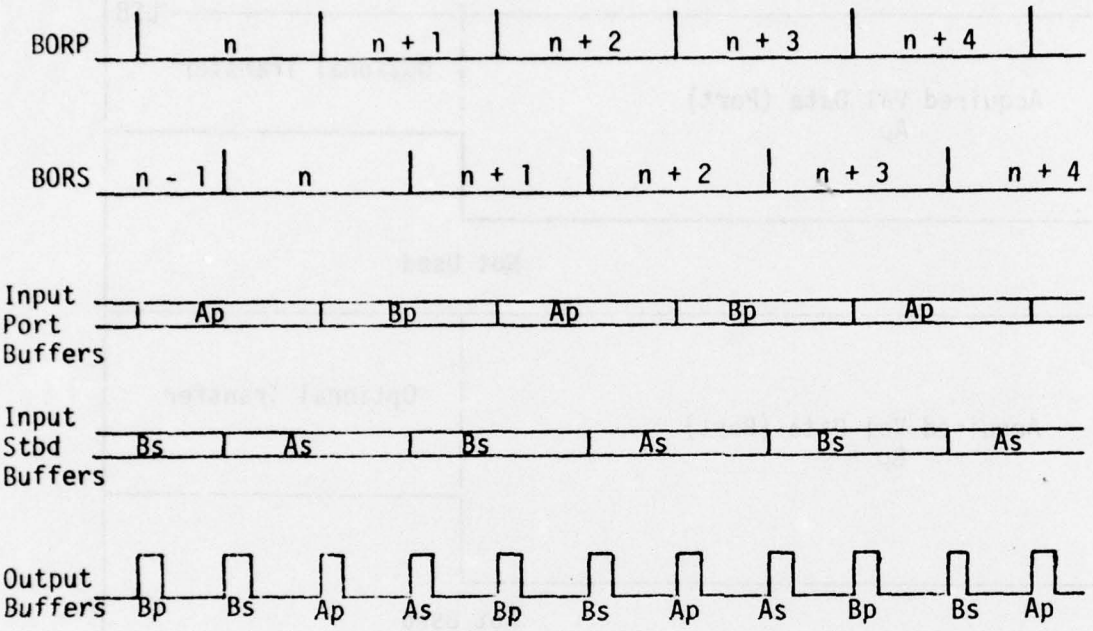


Figure 4.3 Acquisition Data Buffer I/O

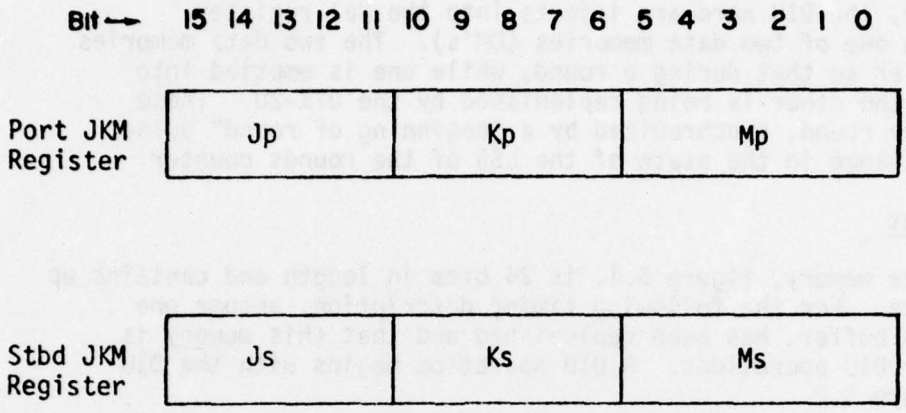


Figure 4.4 Output Format

5. FIRE CONTROL COMPUTER INTERFACE - DIU

For every correct address match from the first 16 words of the address memory, the DIU hardware injects into the Val register data obtained from one of two data memories (DM's). The two data memories form a double buffer so that during a round, while one is emptied into the Val register, the other is being replenished by the UYK-20. These roles reverse every round, synchronized by a "beginning of round" pulse derived from the change in the state of the LSB of the rounds counter.

5.1 Val Input

Each data memory, figure 5.1, is 24 bits in length and contains up to 16 words of data. For the following timing description, assume one data memory, the B buffer, has been replenished and that this memory is now accessible for DIU operations. A DIU operation begins with the DIU enable pulse, figure 5.2.

If at the time of the match, the F/S address bit in that location was found to be 0 (first address) the following events occur:

a) Loc 15 (relative address within the B buffer) of the data memory is addressed, and its contents are made available for the entire duration of the DIU enable pulse. The address lines from the address memory are made available to the data memory for this purpose (the data memory contains Val input data which sequentially corresponds to the positions counter values stored in the address memory).

b) $\overline{bg}$ goes low, on the positive edge of the Uph pulse, disabling the variables/constants memory from being loaded into Val with the A pulse. $\overline{bg}$ goes high again on the negative edge of the Ad' pulse.

c) The iIL pulse is generated, synchronous with and for the same duration as the A pulse, causing the data from location 15 of the data memory to be loaded into the Val register.

If the F/S address bit had been 1 (second address):

a) $\overline{bg}$ would go low at the negative edge of the B pulse and would return to the high state at the negative edge of the Cd' pulse.

b) The iIL pulse would be generated, coincident with the C pulse, loading the data from location 15 into the Val register.

Note: The data from location 15 had been preloaded as that to be injected from a first or second address. It therefore corresponds to the state of the F/S add. bit. No provision is made for doing DIU's for both the first and second address of the same instruction.

5.2 Replenishment

Replenishment of the inactive data memory is done by successive double word transfers from the UYK-20 computer. Synchronized with the beginning of a round, the UYK-20 receives a port or starboard interrupt along with the new round number. The UYK-20 then at its convenience initializes a data-out chaining program to fill the data memory made currently inactive.

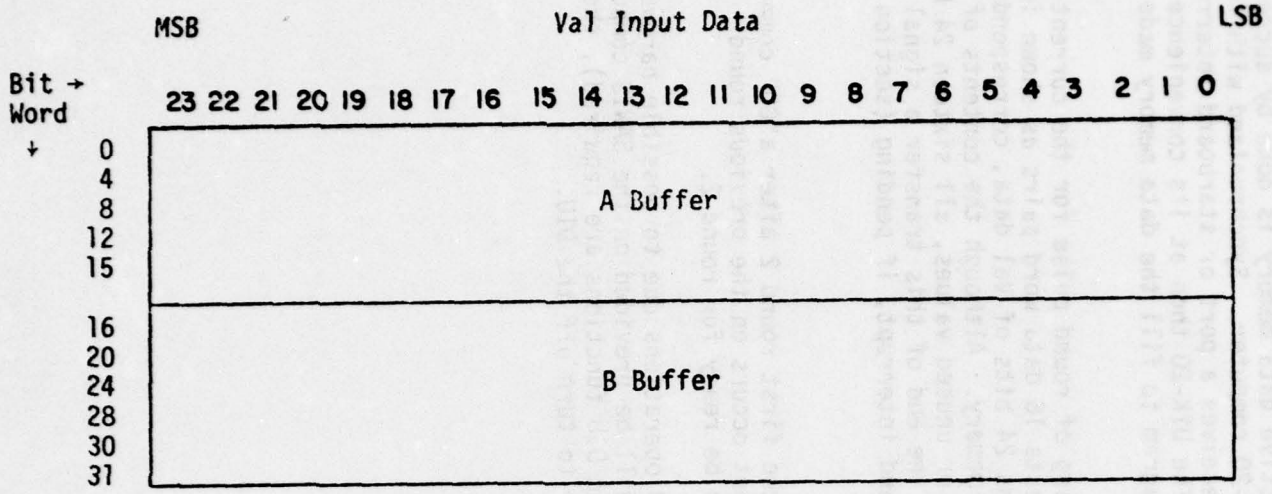
At the same time (beginning of round pulse for the current round) the DIU hardware sequentially requests 16 data word pairs as shown in figure 5.3. Each of these word pairs forms 24 bits of Val data, corresponding to the M-22 address stored in the address memory. Although the contents of the Data Memory may contain static, dynamic or unused values, all sixteen 24 bit locations are replenished by the UYK-20. At the end of this transfer a signal is generated to enable the next beginning of round interrupt, if pending (section 6).

5.3 Start Up

DIU operations begin on the first round 2 after a "GO" command (section 6) is issued. Replenishment occurs on the previous round (round 1), allowing the A buffer to be ready for round 2.

Note that to prevent accidental DIU operations due to possible hardware faults, a disable switch and warning lamp will be provided on the SAWIS computer rack. During live missile firings (when no DIU functions are required), the SAWIS software will instruct the operator to turn off the DIU.

UNCLASSIFIED



UNCLASSIFIED

Figure 5.1 DIU Data Memory

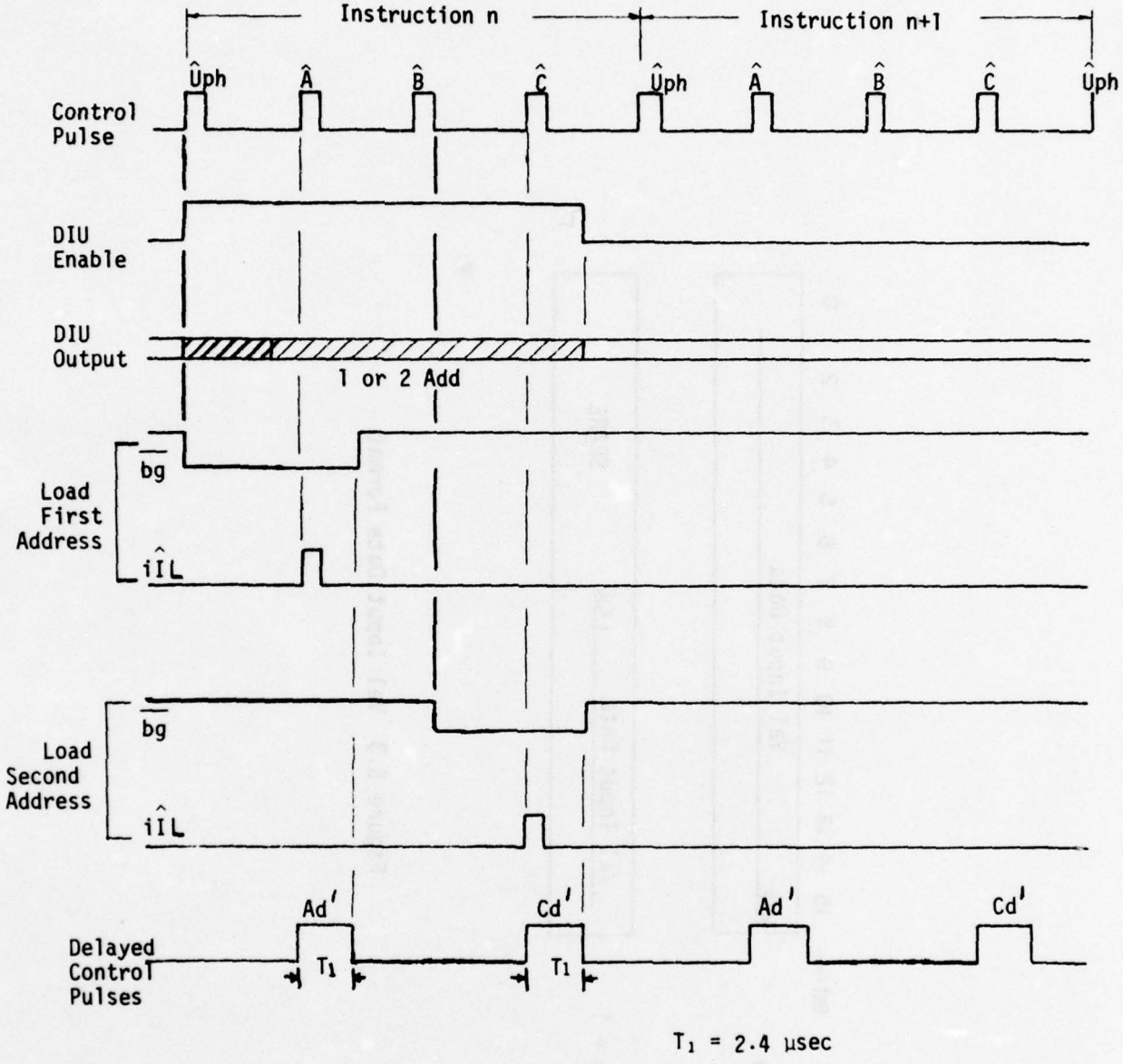


Figure 5.2 DIU Timing

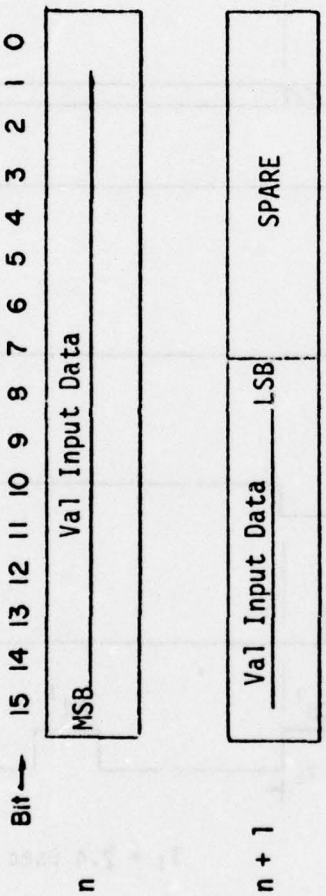


Figure 5.3 Val Input Data Format

6. FIRE CONTROL COMPUTER INTERFACE - INTERRUPT AND INSTRUCTION HARDWARE

6.1 UYK-20 I/O - Chaining Programs

As described in the previous sections, data associated with the port or starboard fire control computers flows to and from the UYK-20 computer. All data I/O interacts with predefined buffers in the UYK-20 memory. These buffers are made accessible to the UYK-20 I/O controller by the operation of input and output chaining programs. The I/O controller executes the chaining program, which in turn initializes the I/O controller with the starting address of the buffer and a word count equal to the buffer length. Chaining programs also perform other functions such as generating interrupts to the processor when the word count reaches zero, allowing automatic initialization of double buffers, etc. The full usage of chaining programs will be described in Section 8. An NTDS fast I/O channel is used, where there are 4 types of data transfers available: input data, output data, external interrupt and external function. Data from the Acquisition Buffer is of the input data type, data to the DIU data memory is of the output data type. These transfers occur to and from many core buffers, the addresses of which must be initialized at the beginning of each of the port and starboard rounds.

6.2 UYK-20 - External Interrupt

An external interrupt is generated for the port and starboard beginning of rounds markers.

For these interrupts (which are generated by asserting the external interrupt request line on the I/O channel) an interrupt code word is placed on the input data lines. This code word is stored in a specific core location and is accessed during the interrupt service routine for that channel.

The format for this code word is specified in figure 6.1. Bits 0 and 1 contain the codes, BORP and BORS. For these interrupts, bits 8-11 contain the associated round number. When the interrupt is received, the UYK-20 will examine the code word and initiate the execution of software to initialize I/O data transfer chaining programs for the current round. A considerable number of events are controlled and tested during the execution of this software. These will be identified in section 8.

Since only one interrupt for an input channel can be held pending, the interrupt hardware controls all pending external interrupts in the following manner:

a) If a BORP and BORS pulse occur simultaneously, the BORP interrupt will occur first. The other will be held pending (including its code word) until the UYK-20 re-enables the external interrupt for that channel and both the Acquisition data buffer and DIU DM transfers have been completed. The second interrupt then occurs.

b) If during the servicing of one interrupt another occurs, it will be held pending the completion of the first.

6.3 UYK-20 - Forced External Function

Loading and reading of the various memories and registers in the interface hardware as well as run commands to the hardware are facilitated by means of hardware instructions. Any of these instructions are issued to the hardware by means of the execution of a Forced External Function instruction in the UYK-20. The 16 bit data associated with this instruction (a chaining instruction) is applied to the output data lines of the I/O channel. At the same time a pulse appears on the external function enable line, allowing the hardware to store and decode the instruction. There are 11 instructions that are required to initialize and run the hardware. These are outlined in figure 6.2. Bits 8-11 contain a 4 bit code from which 6 out of 11 possible instructions are obtained. Four of these will command the interface hardware to do block I/O data transfers associated with the port and starboard Address Memories in the address recognition hardware.

In each case these memories can be loaded or read, provided the respective output or input chaining program had previously been initiated. For example, if the port address memory is to be loaded, then a chaining program would first be initiated which would allow the interface hardware to request sixty-four 16 bit words from a UYK-20 buffer. The Forced External Function instruction is then executed, commanding the hardware to begin the transfer by transmitting the command word containing 4 in the I/O function code. The interface hardware then takes over and generates 64 data requests to the UYK-20. The first 32 words are loaded into the first sixteen 32 bit words of the port address memory, the remaining 32 words are loaded into the last thirty-two 16 bit words of the address memory. At the termination of this transfer, the interface hardware becomes ready to accept another command.

As shown in this example sixty-four 16 bit word transfers are required to load or read the address memories. No provision is made to do fewer transfers, thus for unused locations the address valid bit will be loaded as 0.

The port and starboard Output Format Registers can also be loaded and read in this manner, except that both 16 bit registers are sequentially accessed. If, for example, the OFR's are to be loaded, a

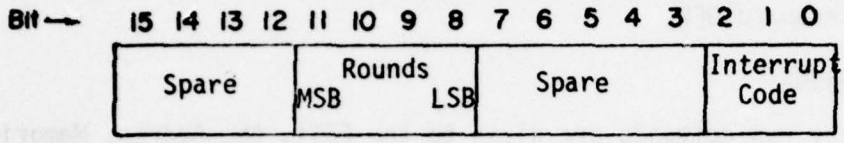
chaining program for a double word transfer would be initiated followed by a load/port OFR command. The interface hardware then requests 2 words from the UYK-20; the first is loaded into the port OFR, the second is loaded into the starboard OFR.

6.4 Run Commands

Before any run commands are given to the FCCI, the Address Memories and the OFR's must be initialized. There are 4 such commands, Acquisition-port, DIU-port, Acquisition-starboard and DIU-starboard. Any or all of these can be initiated by one Forced External Function instruction by setting bits 0-3 respectively to one's. Resetting any of these bits in a subsequent transfer will stop those respective interfaces.

Note: If a power fail occurs, the complete initialization process must be repeated. Data in the Address Memories and the OFR's is lost. There is no provision to make this equipment recoverable during DIU type runs. Thus the software, when detecting a power fail, will terminate the DIU run. For Acquisition runs, the FCCI will be self-recoverable on an M-22 power fail. FCCI power failure will be made coincident with UYK-20 power fail by arranging the mains input to be common to both. Thus, the power fail interrupt within the UYK-20 can be used.

A Reset instruction is provided to set all logic to a predefined state.



Interrupt Code

Bit			Function
2	1	0	
0	0	0	BORP (Beginning of Round - Port)
0	0	1	BORS (Beginning of Round - Stbd)
0	1	0	Spare
			↓
1	1	1	

Figure 6.1 Interrupt Code Word

Bit→	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1 0
	Spare	I/O Functions	Spare	R/S Commands

Table A R/S (Run/Stop) Commands (1 if Run, 0 if Stop)

Bit	Function
0	Acquisition - Port
1	DIU - Port
2	Acquisition - Stbd
3	DIU - Stbd
4	Reset

Table B I/O Functions

Bit	Function
11 10 9 8	
0 0 0 0	No Action
0 0 0 1	Read - Port - AM
0 0 1 0	Read - Stbd - AM
0 0 1 1	Read - Port/Stbd - OFR
0 1 0 0	Load - Port - AM
0 1 0 1	Load - Stbd - AM
0 1 1 0	Load - Port/Stbd OFR
0 1 1 1	Spare
↓	↓
1 1 1 1	Spare

Figure 6.2 Forced External Function Command Word

7. AUXILIARY EQUIPMENT INTERFACE

Although approximately one half of all acquired data is available from the fire control computers, data such as a launcher bearing error, gun sequence signals, etc., must be acquired directly. The following classes of signals have been identified:

a) Analog - Signals within maximum ranges of 50 volts, some with high impedance sources.

b) Status - 24 or 5 volt relay drive signals.

c) Clock - A commercial WWV synchronized clock with 10ms resolution and 3 addressable 16 bit words of TTL compatible data.

d) Video Injection - A signal supplied to the missile, the frequency of which is proportional to the target closing velocity.

e) Gun Sequence Signals - "Status" signals indicating the sequence and timing of shell feed loading.

7.1 AEI Functions

Since interference to the M-22 equipment is not allowed, and due to the relatively long distances between the M-22 equipment and the AEI, the following are the input characteristics and functions of the AEI:

a) Analog - Input amplifiers are of two types, low gain (0.16) and unity gain. Both types are differential and provide scaling and filtering to provide signals compatible to the A/D converter.

b) Status - Including gun sequence signals, these will be buffered by opto isolators.

c) Clock - The clock is interfaced to the AEI by means of an Auxiliary Function Interface to be described later.

d) Video Injection - A frequency counter is employed in 2 other Auxiliary Function Interfaces to provide the frequency of the port and stbd VI signals.

e) Gun Sequence - These status signals are processed by another Auxiliary Function Interface.

Since most of these signals are available from equipment located near the missile workshop, the AEI will be located there. However, many of the analog and status signals are associated with the gun, therefore an extension of the AEI will be located in the gun area. Multiplexing of the gun signals will allow a simple bus interconnecting this "remote" interface to the "local" AEI interface.

7.2 AEI Command Word

Each analog, 16 bits of status (local or remote) and each of the Auxiliary Functions are acquired by the UYK-20 by issuing a command word to the AEI interface. The format for this command word is shown in figure 7.1. The 5 functions, table 7.1, are represented by the code in bits F_2, F_1, F_0. For each function, the channel address, bit 0-7, designates each analog channel, status word or auxiliary function. Thus the AEI is expandable up to 256 of each of the 5 functions, although this limit far exceeds the approximate 80 analog channels, 10 status words and 4 auxiliary functions. Table 7.2 defines the channel number for each of the 4 auxiliary functions.

If an analog function is selected, bits 12 and 11 (A_1A_0) specify the full scale input sensitivity of the Selected Analog Channel. If an input amplifier with a gain of 1 had been selected, then for A_1, A_0 = 00, the full scale input sensitivity will be ± volt. For A_1,A_0 = 01, 10 or 11, the input sensitivities will be ±2, ±4 or ±8 volts respectively. For amplifiers with gains of 0.16, multiply the above full scale sensitivities by 5.

Since these commands must be individually given to the AEI, those which are required are pre-stored in a command buffer in the UYK-20. Each word is requested by the AEI through the I/O channel. An output chaining program is employed to access the command buffer. To start the process a Forced External Function instruction is given (no significant data need be transferred since the AEI will need only the pulse on the External Function Acknowledge line to begin its operation). The AEI then requests the first command word. When the data becomes available (e.g., A/D conversion is complete), the AEI generates an input data request to the UYK-20. The resultant is stored in a buffer accessed by an input chaining program. The AEI then requests another command word. This process repeats until the command buffer has been completely read.

In this manner any number of AEI signals may be acquired with the execution of only one Forced External Function instruction. A chaining program interrupt signals the UYK-20 that the entire AEI operation is complete.

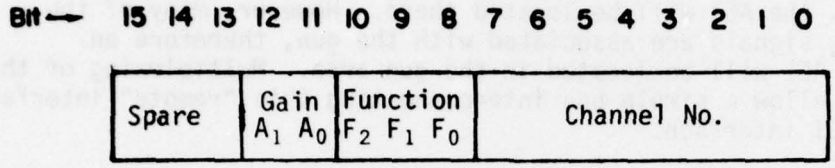


Figure 7.1 AEI Command Word

Table 7.1 AEI Functions

Function			Source and Location
F_2	F_1	F_0	
0	0	0	Analog - Local
1	0	0	Analog - Remote
0	0	1	Status - Local
0	1	0	Status - Remote
0	1	1	Auxiliary

Table 7.2 Auxiliary Functions

Channel No.	Auxiliary Functions
0	Clock
1	Video Injection - Port
2	Video Injection - Stbd
3	Gun Sequence Interface
4 ↓ 15	Spare ↓ Spare

8. FCCI AND AEI CONTROL SOFTWARE

The following software descriptions define the required procedure for initialization and operation of the FCCI and AEI interfaces. It is not intended that these descriptions represent the actual configuration that will exist since it is recognized that this structure must fit into what is realizable within the confines of the NAVELEX Level 2 and SDEX software.

8.1 Initialization

Prior to initiating the Run Mode several parameters must be initialized. Refer to figure 8.1 and Table 8.1.

For data acquisition a hardware Address Memory must contain predefined addresses for a particular run. First a core buffer (ADMBUF) is set up with these predefined addresses. Then, an output chaining program is initiated with a buffer address pointer of ADMBUF and a word count of 64. When a Forced External Function Command is given to load the Address Memory, transfer takes place from ADMBUF to the Address Memory without any CP action. When the word count becomes zero the chaining program halts. If required the CP can check a flag indicating that the transfer is finished.

The above procedure is used to preload the Address Memory associated with the port M-22 computer and is repeated to preload the Address Memory associated with the starboard M-22 computer.

Acquisition data transfers may be double or single word length. Three parameters J,K and M, which are location pointers for the Address Memory, are used to control the data transfers. These are defined as follows:

K - Address of first word transfer,
J - Address of first single word transfer,
M - Address of last word transfer.

During initialization two hardware output format registers are preloaded. This is accomplished by setting up a 2 word core buffer (JKMPS) containing J, K and M for port and starboard respectively. An output chaining program is initiated with a buffer address pointer of JKMPS and a word count of 2. A Forced External Function Command is then given to load the data format registers. Section 4.4 of the report discusses the output format registers.

For DIU operation 4 core buffers must be initialized with dynamic and static DIU data for a complete set of rounds. DBUFP1 and DBUFP2 are associated with port M-22 computer while DBUFS1 and DBUFS2 are associated with starboard M-22 computer. Double buffering is used to allow replenishing of dynamic values for the next set of rounds while the current set of dynamic and static values is being transferred to the hardware Data Memories round by round. DIU buffer format is shown in Figure 8.4 and the data format is as shown in Figure

5.3 for Val Input Data Format. No initialization of the Data Memories is required because the Fire Control Computer Interface will not allow DIU operation to start until the first round 2 interrupt has occurred. By this time DIU data corresponding to round 2 would have been loaded into the appropriate DM at round 1 interrupt.

Two 41 word core buffers associated with A/D, Status and Clock must be initialized before run time. ADSTOP (A/D and Status Output Port) and ADSTOS (A/D and Status Output Starboard) are filled with command words. The format of these command words is described in the hardware section of this report.

At this time appropriate interrupts could be enabled in preparation for the RUN Command.

8.2 Acquisition

Any reference to acquisition usually refers to data from the Fire Control Computer Interface. A/D, Status, Clock and Video Injection signals obtained from the Auxiliary Equipment Interface will also be described in this sub-section as it pertains to the software action to transfer this data to the UYK-20 computer.

All data acquired will be placed in Disk Write Buffers according to the format shown in Figure 8.3. A double buffer, each a maximum of 2K words, is provided for each associated M-22 computer such that while one buffer is being filled the other can be written to the disk.

After a RUN Command has been given the UYK-20 computer waits for an interrupt. The first "beginning of round" interrupt will be for round one.

The following sequence of events takes place when a beginning of round interrupt occurs. By inspecting the Interrupt Code Word we first determine if it is a BORP (beginning of round port) or a BORS (beginning of round starboard) and then we determine the round number. Figure 8.2 illustrates the procedure for BORP. For BORS use the appropriate buffer address pointers and the same procedure.

If it is round one the disk write buffers are switched to give us the correct BASE address (see figure 8.3) for filling the next disk write buffer.

If it is round one and not the first set of rounds, a disk write operation is initiated. If a disk operation is in progress at this time the request is held pending and the disk operation will be initiated during the disk interrupt service routine which is entered when a disk operation is completed.

If it is not round one, BAP's (buffer address pointers) for storing data from the Fire Control Computer Interface and the Auxiliary Equipment Interface are incremented.

For acquisition of data for the previous round, an input chaining program (no interrupt) is initiated with a BAP and word count as calculated in figure 8.3.

While acquisition data is transferring, A/D and Status transfer is initiated. An output chaining program (no interrupt) is initiated with a BAP of ADSTOP and a word count that is predetermined for a particular run. An input chaining program (with interrupt when complete) is initiated with a BAP and word count as shown in figure 8.3. A F.E.F. command is now given to start A/D and Status transfer. If a transfer is already in progress the request is held pending and the transfer will be initiated during the input chain interrupt service routine.

At the end of the BORP interrupt service routine the appropriate interrupts are enabled and an exit from the routine is executed.

8.3 DIU

If DIU is indicated in the RUN command operations are synchronized with the "beginning of round" interrupt. Refer to figure 8.2.

After BORP, at a time determined by the hardware interface, the hardware transfers DIU DM into the VAL register. Initially this does not happen until the first round two. The DM at this time contains round n (current round) information which was replenished during the previous round from the appropriate DIU Buffer. Refer to figure 8.4.

If it is round one the DIU buffers are switched to give the correct BASE address (see figure 8.4) for replenishing the DM.

If it is round one and not the first set of rounds, replenishing of dynamic values for the next set of rounds in the alternate DIU buffer is initiated.

If it is not round one, the buffer address pointer is incremented in preparation for loading DIU data into the DM.

Within the BORP interrupt routine the software initiates the transfer of round n + 1 information to the hdwr DM (A or B). This transfer is started by initiating an output chaining program (no interrupt) with a BAP and word count (32) as shown in figure 8.4.

For BORS operation use the appropriate buffer address pointers and the same procedure as above.

BUFFER NAME	WORDS	DESCRIPTION
ADMBUF	64	ADDRESS MEMORY BUFFER
DBUFP1	512	DUI BUFFER PORT 1
DBUFP2	512	DIU BUFFER PORT 2
DBUFS1	512	DIU BUFFER STBD 1
DBUFS2	512	DIU BUFFER STBD 2
DSKWP1	2K	DISK WRITE PORT 1
DSKWP2	2K	DISK WRITE PORT 2
DSKWS1	2K	DISK WRITE STBD 1
DSKWS2	2K	DISK RITE STBD 2
ADSTOP	41	A/D & STATUS OUTPUT PORT
ADSTOS	41	A/D & STATUS OUTPUT STBD
JKMPS	2	J,K,M, PARAMETERS FOR PORT & STBD

TABLE 8.1 CORE STORAGE ALLOCATION

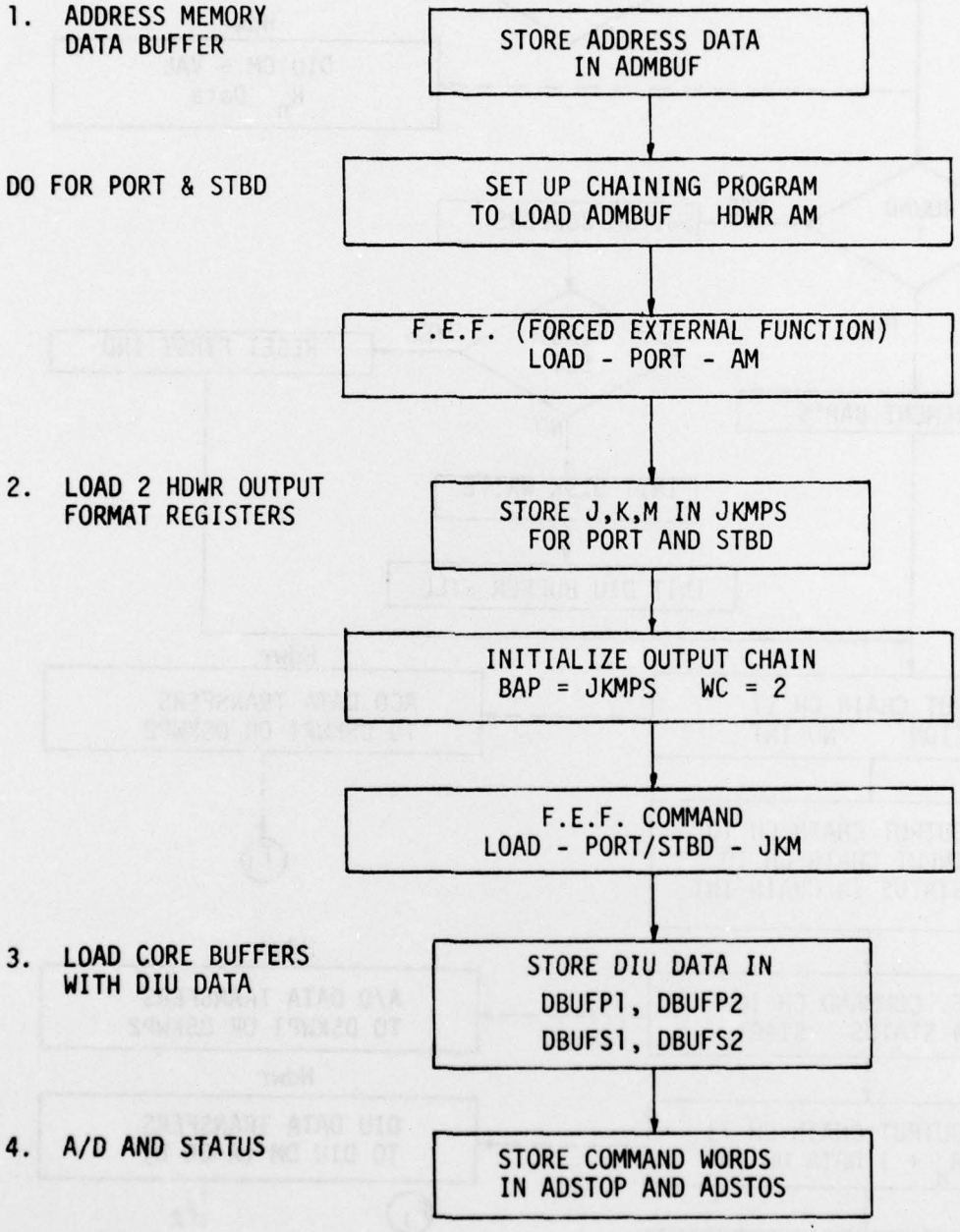


FIGURE 8.1 INITIALIZATION

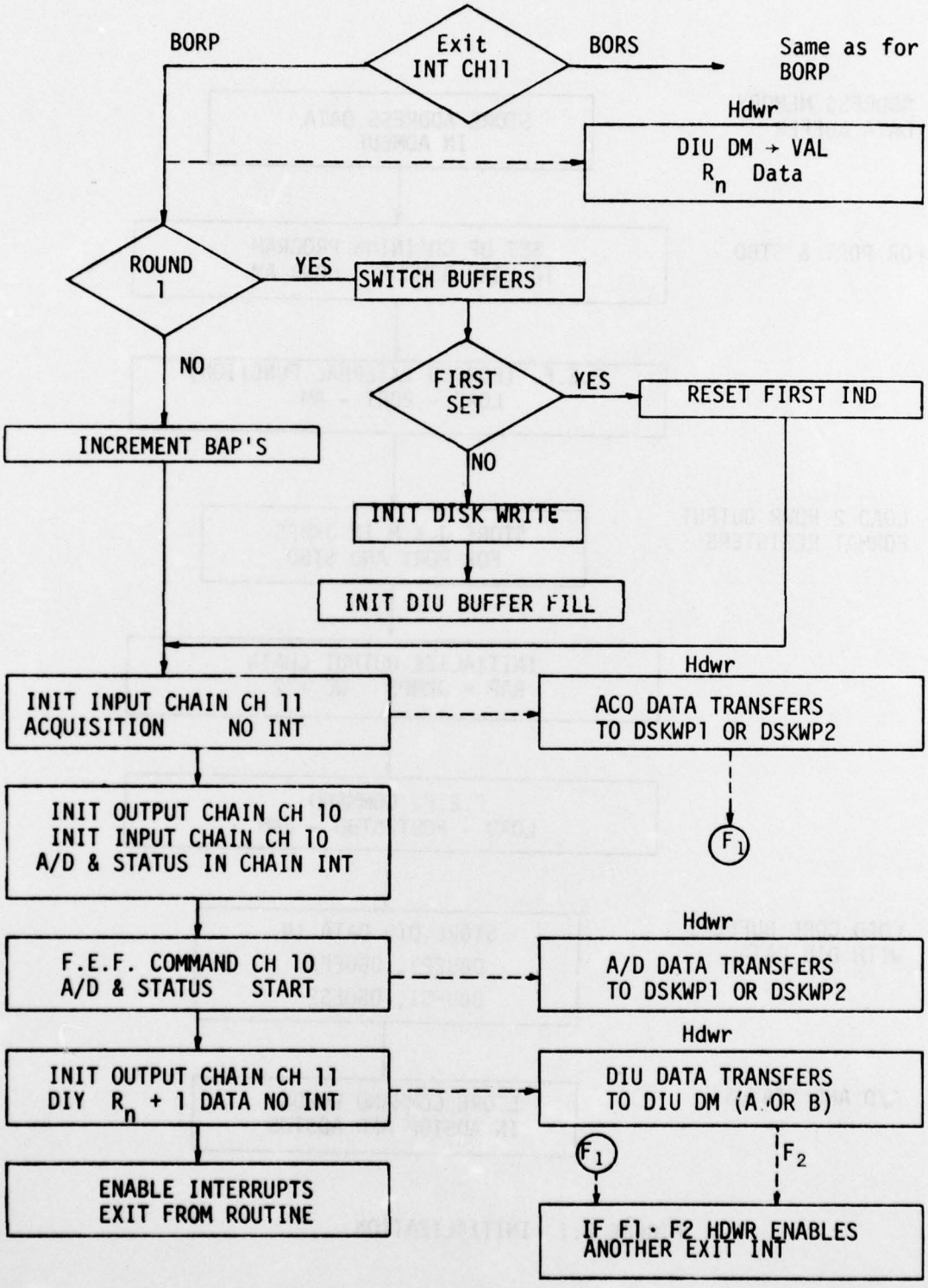
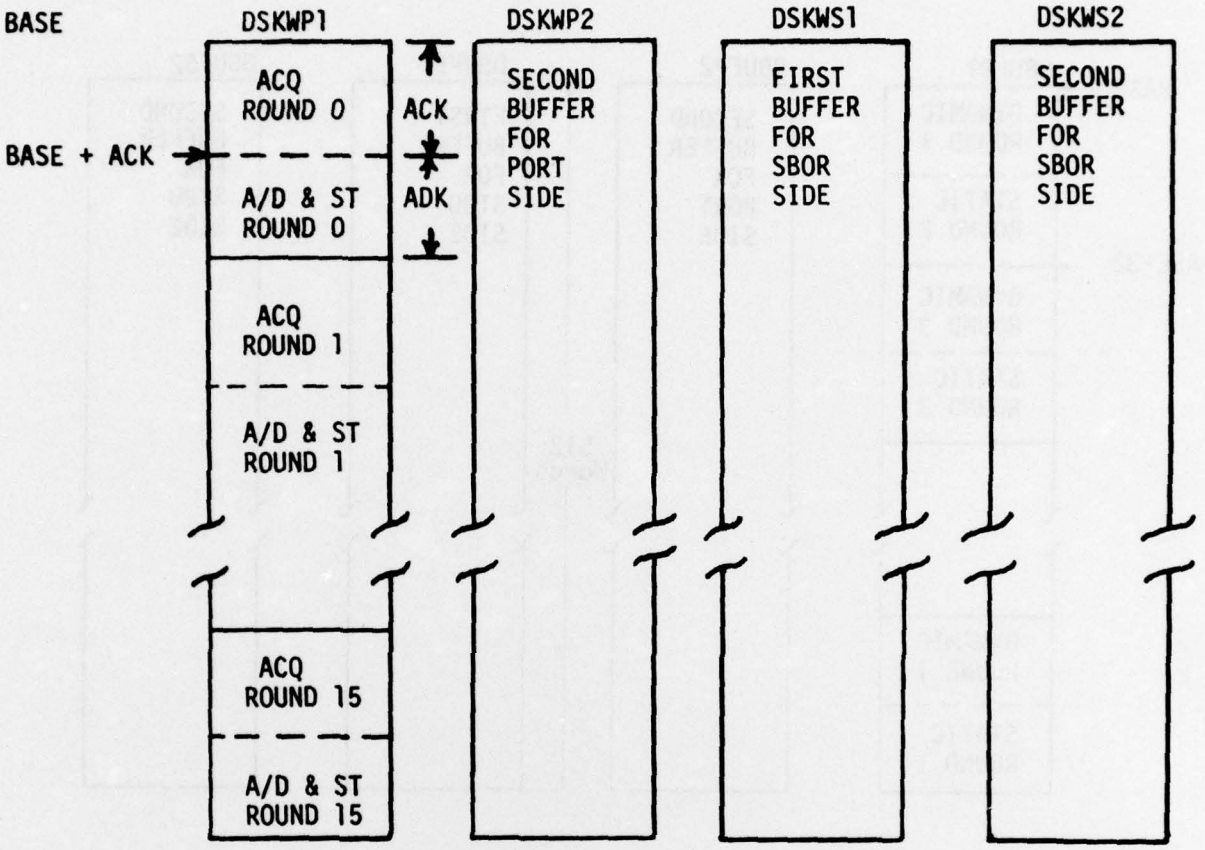


FIGURE 8.2 BOR SEQUENCE OF EVENTS



BAP (ACQ) = BASE + ((Rn-1) AND 15) (ACK + ADK)

BAP (A/D) = BASE + ACK + ((Rn-1) AND 15) (ACK +ADK)

BASE = ADDRESS OF APPROPRIATE DISK WRITE BUFFER

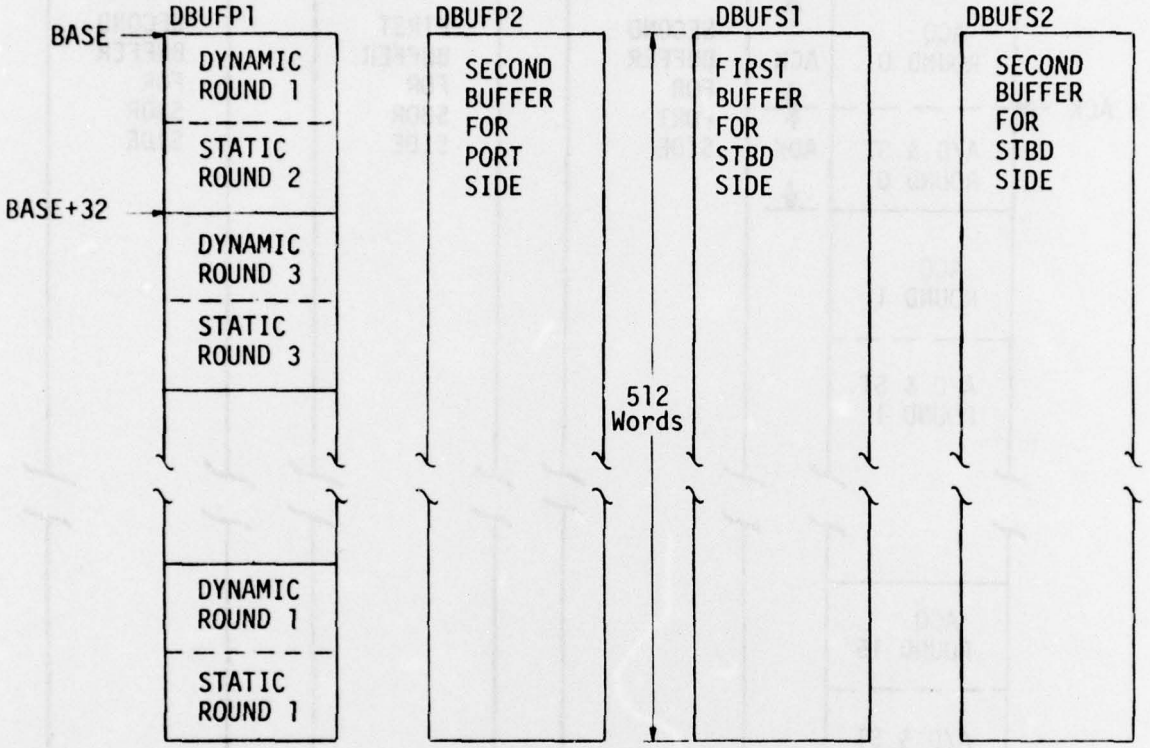
Rn = CURRENT ROUND NUMBER

ACK = NO. OF ACQ WORDS = 2(J-K) + (M-J+1)

ADK = NO. OF A/D & ST WORDS (PREDETERMINED)

WC FOR DISK WRITE = 16(ACK+ADK)

FIGURE 8.3. DISK WRITE BUFFER FORMAT



BAP = BASE + 32((Rn-1) AND 15)

BASE = ADDRESS OF APPROPRIATE DIU BUFFER

Rn = CURRENT ROUND NUMBER

WC FOR DM REPLENISHMENT = 32

FIGURE 8.4 DIU BUFFER FORMAT

REFERENCES

1. Canadian Sea Sparrow Close Range Missile System (System Manual), Vol 8. System Functional Data - System Functional Drawing Part 1 and Part 2

2. Users Handbook for AN/UYK-20(V) Computer Support Software

a)	Vol 1 Level 1, Level 2	NAVELEX 0967-LP-598-2010
b)	Vol 2 SDEX/20	NAVELEX 0967-LP-598-2010
c)	Vol 3 Hardware, Assembler, Fortran	NAVELEX 0967-LP-598-2030
d)	Vol 4 CMS-2M	NAVELEX 0967-LP-598-2040

3. AN/UYK-20 Technical Description Sperry-Univac

4. AN/UYK-20 Specifications Sperry Univac

Part 1	SB-10161
Part 2	SB-10592
	SB-10631
	SB-12407
	DS 4772

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13. ABSTRACT

This report describes the hardware and software related concepts of SAWIS-280. A simplified description of the Surface and Air Weapons Control System is presented in the Introduction showing a need for a computer based performance monitoring/analysis system. Technical details of the relevant portions of the WM-22/6 Fire Control System are described as a base point for the design of two system interfaces. Also described in detail are the following: Fire Control Computer Interface, Auxiliary Equipment Interface and FFCI and AEI Control Software.

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